UNIVERSIDADE ESTADUAL DE CAMPINAS
Faculdade de Engenharia Elétrica e de Computação

Mateus Biancarde Castro

Reconfigurable Sigma Delta Modulator for Analog-to-Digital Converters in Multi-Standard Wireless Receivers in 65-nm Process

Modulador Sigma Delta Reconfigurável para Conversor Analógico-Digital em Receptores Wireless Multi-Padrão em Processo de 65-nm

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Dissertação apresentada à Faculdade de Engenharia Elétrica e de Computação da Universidade Estadual de Campinas como parte dos requisitos para a obtenção do título de Mestre em Engenharia Elétrica, na área de Eletrônica, Microeletrônica e Optoeletrônica.

Dissertation presented to the Faculty of Electrical and Computer Engineering of the University of Campinas in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the area of Microelectronics.

Supervisor/Orientador: Prof. Dr. Leandro Tiago Manêra
Co-supervisor/Coorientador: Eduardo Rodrigues de Lima, PhD

Este trabalho corresponde à versão final da Dissertação defendida por Mateus Biancarde Castro e orientada pelo Prof. Dr. Leandro Tiago Manêra.

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Título da Tese: "Reconfigurable Sigma Delta Modulator for Analog-to-Digital Converters in Multi-Standard Wireless Receivers in 65-nm Process"

Prof. Dr. Leandro Tiago Manêra (Presidente)
Prof. Dr. Fernando Rangel de Sousa
Prof. Dr. Fabiano Fruett

A ata de defesa, com as respectivas assinaturas dos membros da Comissão Julgadora, encontra-se no SIGA (Sistema de Fluxo de Dissertação/Tese) e na Secretaria de Pós-Graduação da Faculdade de Engenharia Elétrica e de Computação.

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Resumo

Com o crescente número de padrões de comunicação sem fio nas últimas décadas, reconfigurabilidade de transceptores se torna um recurso interessante e benéfico em dispositivos embarcados System-on-Chip (SoC) que necessitam de uma grande variedade de padrões de Radiofrequência (RF) para processamento de sinais. Com o objetivo de desenvolver um transceptor totalmente reconfigurável, que é capaz de operar em vários padrões com consumo de potência adequado, a reconfigurabilidade de blocos individuais do transceptor se torna um assunto atraente para pesquisa. Especificamente no caso de Conversores Analógico-Digitais (ADCs), a topologia de ADC ΣΔ mostra algumas vantagens com relação a reconfigurabilidade com o objetivo de redução no consumo de potência na faixa de baixas frequências de operação. Este tipo de topologia permite modificações como a redução da frequência de amostragem, a ordem da formatação de ruído e o número de bits do quantizador de saída, tudo em troca da resolução e consumo de potência. O principal objetivo deste trabalho é apresentar o projeto completo de um ADC reconfigurável que opere na faixa de baixas frequências de comunicações móveis sem fio, especificamente GSM (banda de 200 kHz) e UMTS (banda de 2 MHz), e adicionalmente fornecer a operação para Bluetooth com banda de 500 kHz, juntamente com o projeto de um sintetizador de clock baseado em Phase Locked Loop (PLL) para a síntese das frequências de sobreamostragem necessárias para a operação do modulador. Todo o trabalho segue a metodologia top-down/bottom-up, incluindo o desenvolvimento de macro-modelos, implementação a nível de transistor e implementação parcial de layout. Todo projeto de sub-circuitos e modelos em Verilog-A é detalhado, incluindo o amplificador operacional de transcondutância, comparadores, quantizador de 5 níveis, chaves, sintetizador de clock, detector de fase e frequência, bomba de carga, filtro, oscilador controlado por tensão, divisor de frequência N-inteiro e gerador de correntes de polarização. O resultado de cada um dos principais sub-circuitos é destacado. O modulador proposto opera para GSM (banda de 200 kHz), Bluetooth (banda de 500 kHz) e UMTS (banda de 2 MHz), atingindo um número efetivo de bits de 11,51, 10,16 e 8,82 respectivamente, com um consumo de 10,8, 10,8 e 14,5 mW respectivamente e uma figura de mérito de Schreier de 145, 140 e 145 respectivamente. A maior contribuição do trabalho é o design completo e integração de ambos o modulador ΣΔ reconfigurável e do sintetizador de clock.

Abstract

With the rising number of wireless communication standards in the past decades, transceiver reconfigurability becomes an interesting and beneficial feature in System-on-Chip (SoC) embedded devices that require a large variety of Radio Frequency (RF) standards for signal processing. With the aim of developing a fully reconfigurable RF transceiver, that is able to operate in several standards with adequate power consumption, the reconfigurability of the individual building blocks is an enticing research subject. Specifically in the case of the Analog-to-Digital Converters (ADC), the ΣΔ ADC topology shows a few advantages in regards to reconfigurability with the goal of power consumption reduction in the lower frequency range of operation. This type of topology allows for the reduction of the sampling frequency, the order of the noise shaping and the number of bits in the output quantizer, all in exchange of resolution and power consumption. The main goal of this works is to present the complete design of a reconfigurable ADC that operates in the lower frequency range of mobile wireless communications, specifically GSM (200 kHz bandwidth) and UMTS (2 MHz bandwidth), and additionally provide the operation for Bluetooth with 500 kHz bandwidth, alongside the design of clock synthesizer based Phase Locked Loop (PLL) for the synthesis of the necessary oversampling frequencies for the modulator. This work follows the top-down/bottom-up methodology, including macro-model development, transistor-level and partial layout implementation. Every sub-circuit design and Verilog-A code is detailed, including the operational transconductance amplifier, comparators, 5-level quantizer, switches, clock synthesizer, phase and frequency detector, charge pump, loop filter, voltage-controlled oscillator, N-integer frequency divider and bias currents generator. The results of each of the main sub-circuits is highlighted. The proposed modulator operates for GSM (bandwidth of 200 kHz), Bluetooth (bandwidth of 500 kHz) and UMTS (bandwidth of 2 MHz), achieving an effective number of bits of 11.51, 10.16 and 8.82 bits respectively with a power consumption of 10.8, 10.8 and 14.5 mW respectively and achieving a Schreier Figure of Merit of 145, 140 and 145 respectively. The major contribution of this work is the complete design and integration of both the reconfigurable ΣΔ modulator and the clock synthesizer.

List of Figures

List of Acronyms

ΣΔM	ΣΔ Modulator
AD	Analog-to-Digital
ADC	Analog-to-Digital Converters
BT	Bluetooth
CIC	Cascade-Integrator-Comb
CMFB	Common-Mode Feedback
CP	Charge Pump
CT	Continuous Time
DAC	Digital-to-Analog Converter
DCL	Digital Cancellation Logic
DMP	Dual Modulus Prescaler
DOTB	Dynamic-Offset Test-Bench
DR	Dynamic Range
DSP	Digital Signal Processor
DT	Discrete Time
DVB-S2	Digital Video Broadcasting - Satellite - Second Generation
ENOB	Effective Number of Bits
EOC	End of Conversion
EVM	Error Vector Magnitude
FF	Fast-Fast
FIR	Finite Impulse Response
FoM	Figure-of-Merit
GBW	Gain-Bandwidth
GPS	Global Positioning System
GS/s	Giga Samples per Second
GSM	Global System for Mobile Communications
IBN	In-Band Noise
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
IoT	Internet-of-Things
ISSCC	International Solid-States Circuits Conference
LF	Loop Filter
LNA	Low-Noise Amplifier
LR	Line Regulation
LTE	Long Term Evolution
LTE-A	Long Term Evolution-Advanced
MASH	Multi-Stage Noise Shaping
MC	Modulus Control

MSB	Most Significant Bit
NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PAR	Peak-to-Average-Power Ratio
PC	Program Counter
PDF	Probability Density Function
PDF	Probability Density Function
PFD	Phase and Frequency Detector
PGC	Programmable Gain Control
PSFD	Pulse-Swallow Frequency Divider
RF	Radio Frequency
RF	Radio Frequency
S&H	Sample-and-Hold
SAR	Successive Approximation Register
SC	Swallow Counter
SDR	Software Defined Radio
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SoC	System-on-Chip
SR	Slew-Rate
SS	Slow-Slow
STF	Signal Transfer Function
TC	Temperature Coefficient
TT	Typical-Typical
UMTS	Universal Mobile Telecommunications System
VCO	Voltage Controlled Oscillator
W-CDMA	Wide-Band Code-Division Multiple Access

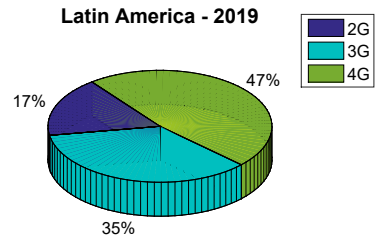
Contents

Chapter 1

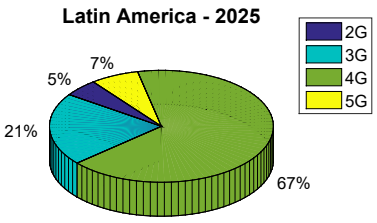
Introduction

With the rising number of wireless standards in the past decades either with the evolution and wide adoption of Bluetooth (BT) and Global Positioning System (GPS) in mobile devices, the continuous use of 2G and 3G technology, popularization of 4G technologies and the recent introduction of 5G in commercial products, transceiver reconfigurability becomes an interesting and beneficial feature in System-on-Chip (SoC) embedded devices that require a large variety of Radio Frequency (RF) standards for signal processing.

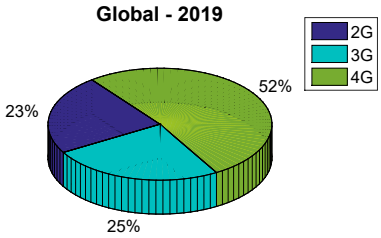
Although smartphones and other communication devices (Internet-of-Things (IoT) devices, GPSs devices, etc.) support a large number of wireless communication protocols, every new standard usually utilizes a dedicated RF module and the innovation in the receiver/transmitter (excluding the Digital Signal Processor (DSP)) stays within the reduction of the Integrated Circuit (IC) technology process node size (MORGADO; RIO; ROSA, 2011). For example, in the reverse engineering work of (EVERYTHINGRF, 2019), the disassembly of the iPhone 11 shows at least 7 RF modules, such as Bluetooth, Wi-Fi, Wide-Band Code-Division Multiple Access (W-CDMA) and Long Term Evolution-Advanced (LTE-A). Besides, the standards from 2G and 3G still retain almost 50% of the usage of mobile networks, and it is expected that in 2025 the combination of 2G, 3G and 4G still retain 80% of all mobile network usage, both in the world and in Latin-America as shown by the graphs of Fig. 1.1 (GSMA, 2021). In summary, receivers that meet bandwidth specifications of the newer technologies while also providing backwards compatibility with older generations supply effective demands of the market (BETTINI et al., 2015), while also providing an easy all-in-one receiver front-end IC solution for prototyping discrete applications that require different wireless standards with efficient power consumption.



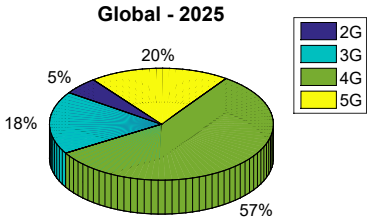
(a) Latin America - 2019.



(b) Latin America - 2025.



(c) World - 2019.



(d) World - 2025.

Figure 1.1: 2G, 3G, 4G and 5G utilization in 2019 and forecast for 2025. (GSMA, 2021).

Predicting the rising number of wireless communication standards, the paradigm of Software Defined Radio (SDR) was conceived (III; GERALD Q. MAGUIRE, 1999) (Fig. 1.2a), where, for the receiver, the signal is captured by the antenna and immediately converted by an ADC and is completely processed digitally, or for the transmitter case, the digital signal is directly converted by a Digital-to-Analog Converter (DAC) amplified by a Power Amplifier (PA) and transmitted by the antenna. The ideal SDR remains impractical due to the unfeasible analog-to-digital and digital-to-analog requirements with conversions ranging from 800 MHz to 300 GHz with high resolutions. For this reason the analog/RF front-end of a SDR was transformed into the reconfigurability and adaptability of the analog signal processing steps, as depicted in Fig. 1.2b, where each of the sub-circuits of the receiver are reconfigurable (MORGADO; RIO; ROSA, 2011). A reconfigurable wireless receiver presents an architecture identical to a standard direct conversion receiver, with the only difference being in the reconfigurability of each sub-circuit that builds the system as shown in Fig. 1.2b, where LNA stands for Low-Noise Amplifier, PGA is an acronym for Programmable Gain Amplifier and DSP is the Digital Signal Processor.

One of the main bottlenecks of high-speed state-of-the-art receivers and other communication systems is the ADC. However, for lower speed standards from 2G and 3G, such as Global System for Mobile Communications (GSM) (specifically EDGE), or Universal Mobile Telecommunications System (UMTS) (specifically W-CDMA) that require 200 kHz

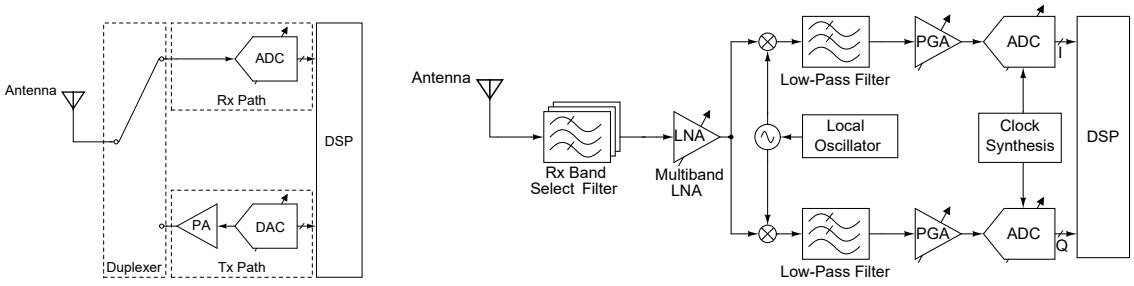


Figure 1.2: Comparison between (a) the ideal SDR and (b) the feasible concept implementation for the receiver (adapted from (MORGADO; RIO; ROSA, 2011)).

and 3.84 MHz bandwidth respectively (considering a direct conversion receiver, these bandwidths are reduced by half (MORGADO; DEL RÍO, et al., 2010)), the ΣΔ ADC topology shows a few advantages in regards to reconfigurability with the goal of power consumption reduction. For example, this type of topology allows for the reduction of the sampling frequency, the order of the noise shaping and the number of bits in the output quantizer, all in exchange of resolution and power consumption. These aspects will be explained in more detail in Sections 2 and 3.

1.1 Justification

Considering the predicted usage of wireless cellular communications in (GSMA, 2021) (Fig. 1.1) and the amount of RF modules seen in modern consumer products as described in (EVERYTHINGRF, 2019), a general purpose, reconfigurable RF transceiver that is power-efficient for each mode of operation becomes an enticing research subject. One possible way of reconfiguration in RF receivers is in the ADC. Specifically, in the case of ΣΔ ADCs its oversampling frequency, order of noise-shaping and number of bits in the quantizer can be adjusted depending on the selected RF standard to be converted with the aim of reducing power consumption, becoming an interesting choice for this type of receivers when operating in the lower frequency range, which encompasses 2G and 3G standards.

1.2 Goals and Contents

Taking into account, the limitations in speed of operation of ΣΔ ADCs, and its advantages in reconfigurability, the main goal of this project is the design of a reconfigurable ΣΔ Modulator

(ΣΔM) for the lower frequency spectrum of operation of mobile wireless communication standards, and the inclusion of Bluetooth with 500 kHz bandwidth, with the purpose of providing a general purpose RF module. Thus, the goal of the project is to design a ΣΔ Modulator for the following standards: 1) GSM (with 200 kHz bandwidth), 2) Bluetooth (with 500 kHz bandwidth) and 3) UMTS (with 2 MHz bandwidth - rounded from 1.92 MHz). The design will follow every step of the analog IC design flow starting with high level simulations in SIMULINK, followed by macro-model simulation with Verilog-A in Cadence's Virtuoso Analog Design Environment, followed by the transistor implementation of every sub-circuit, also in in Cadence's Virtuoso Analog Design Environment and finally the layout implementation of the project in Cadence's Virtuoso Layout Suite.

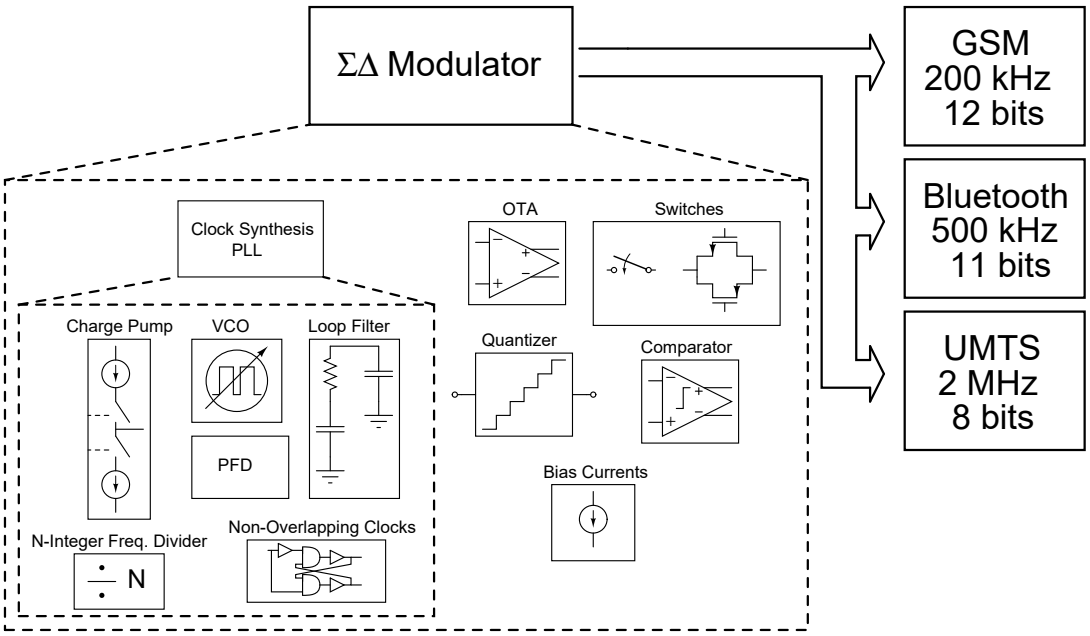


Figure 1.3: Diagram of sub-circuits developed in this work alongside the target standards and specifications.

This work is organized as follows: Chapter 2 will present a detailed bibliography review of analog-to-digital conversion concepts, a review of ΣΔ modulation and ΣΔ ADCs, a brief review of other ADC topologies, followed by a general overview of the current trends in ADC design and examples of reconfigurability in ADCs. Chapter 3 will detail the design steps of every major sub-circuit of the ΣΔM following the top-down/bottom-up methodology, detailing transistor implementation of every sub-circuit (e.g. operational amplifier, quantizers, clock synthesizer, etc.) alongside macro-model implementation in Verilog-A of critical sub-circuits. Chapter 4 will detail the obtained results of the circuits in Chapter 3, highlighting with more

detail the ΣΔM and the clock synthesizer systems. Finally, the conclusions will be presented in Chapter 5.

Chapter 2

Bibliography Review

2.1 Analog-to-Digital Conversion

With the exponential increase of computational power during the past decades, digital-signal processing became the norm for the majority of electronic devices-based applications. However, signals of the real world are analog, meaning that they are continuous both in time and amplitude, and to be processed digitally, a converter is required to transform this signals in digital words, discrete both in time and amplitude. For this reason, ADCs and DACs are essential interfaces between the Digital-Signal Processor (DSP) and the real world analog signals.

The basic concept of a Nyquist-rate Analog-to-Digital (AD) conversion is shown in Fig. 2.1, where the analog signal $v_a(t)$ is initially filtered to suppress any unwanted high frequency components, resulting in v(t). v(t) is, then, sampled by the Sample-and-Hold (S&H) circuit at a rate f_s and is discretized in time resulting in $v_s(n)=v_s(nT_s)$, where $T_s=1/f_s$. Then, the amplitude is quantized by the quantizer block with N bits, to a value closest to the 2^N division of the full-scale input range resulting in $v_c(n)$. Finally, a digital code is assigned to each of the output levels (ROSA, 2018).

The main operations performed by the analog part of the ADC are the sampling and quantization. These operations are a common feature in Nyquist-rate and oversampled ADCs and will be reviewed in the next sections.

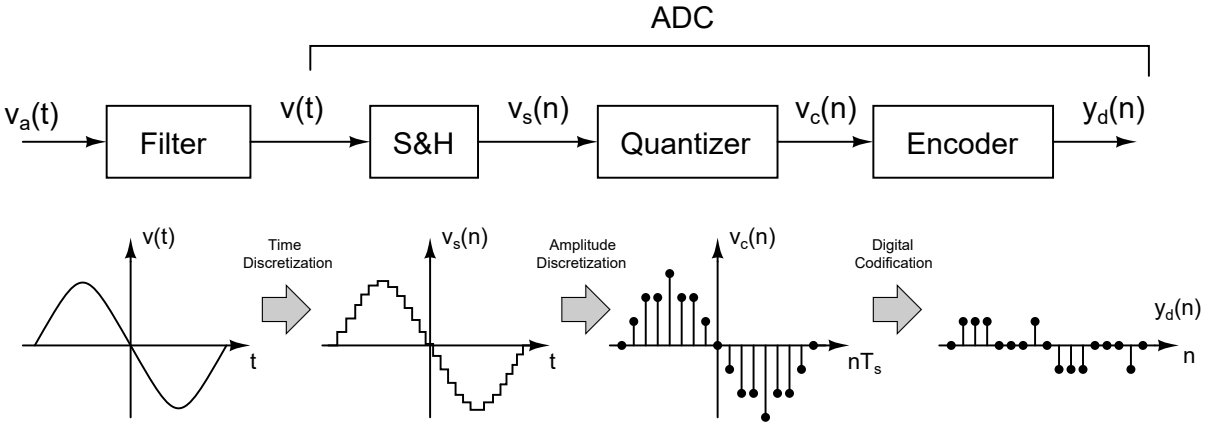


Figure 2.1: Analog-to-Digital conversion diagram for Nyquist rate ADCs (based on (ROSA, 2018)).

2.1.1 Sampling

The sampling operation is performed by periodically sampling the input analog signal in the time domain. The sampling can be represented by the periodic impulse train s(t) or the Dirac impulse train (2.1)

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s). \tag{2.1}$$

Meaning that, the sampled signal representation in the time domain will be given by $v_s(t) = v(t)s(t)$. Thus, the frequency domain representation will be obtained by the convolution of the Fourier transforms of v(t) and s(t), which are respectively $V(f)$ and $S(f)$. The Fourier transform of the impulse train is given by (2.2)

$$S(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} \delta(f - nf_s) \tag{2.2}$$

Since

$$V_s(f) = V(f) * S(f), \tag{2.3}$$

the Fourier transform of the sampled signal will be given by (2.4)

$$V_s(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} V(f - nf_s) \tag{2.4}$$

Fig. 2.2a represents the original signal spectrum where the signal band is equal to $2B$. If sampled with $f_s = 2B$, the resulting spectrum is shown in Fig. 2.2. From this spectrum it is easy to observe the Nyquist-Shannon theorem (PAVAN; SCHREIER; TEMES, 2017) which

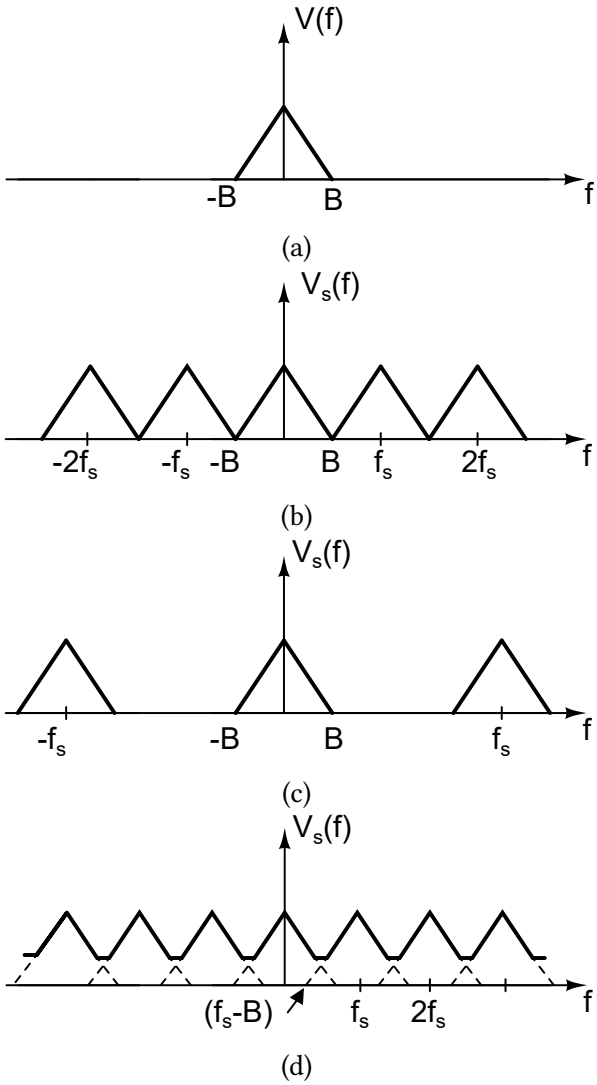


Figure 2.2: Frequency domain representation of (a) original signal; (b) Sampled signal with $f = 2B$; (c) Oversampled signal with $f_s > 2B$; (d) Undersampled signal with $f_s < 2B$.

states that

$$f_s = \frac{1}{T_s} \geq 2B. \tag{2.5}$$

Fig. 2.2c shows a signal sampled in a frequency greater than the Nyquist rate, therefore the signal is considered oversampled. Fig. 2.2d shows a signal sampled in frequency lower than the Nyquist rate, in this case there is an overlap between the spectrum replicas, resulting in aliasing, and the original signal cannot be perfectly recovered.

ΣΔ modulators take advantage in oversampling the original analog signal. In this case the anti-alias filter needed for the signal recovery is relaxed, and the filter design is easier. The ratio in which a signal is oversampled is known as Oversampling Ratio (OSR) and is given by

(2.6) (PAVAN; SCHREIER; TEMES, 2017)

$$OSR = \frac{f_s}{2B} \tag{2.6}$$

where f_s is the sampling frequency and B is the signal bandwidth in Hz.

2.1.2 Quantization

Quantization is a nonlinear memoryless operation where the output y(n) has a staircase characteristic for a given input q(n), that is ideally uniform, so that two adjacent output levels differ by a fixed spacing $\Delta = Y_{FS}/(2^N - 1)$, as depicted in Figs. 2.3c and 2.3d for multi-bit and single-bit quantizer respectively (PAVAN; SCHREIER; TEMES, 2017). The quantizer symbols are shown in Fig. 2.3a for multi-bit quantizers and in Fig. 2.3b for single-bit quantizers.

The difference between the input and output is called quantization error, and is given by e(n) = y(n)-q(n) . Its transfer curve is shown in Figs. 2.3e and 2.3f for multi-bit and single-bit quantizers respectively. Quantizers have a strongly non-linear behavior and a few assumptions have to be made in regards to the nature of the quantization error (PAVAN; SCHREIER; TEMES, 2017) reaching the conclusion that e(n) is assumed to be an additive "noise" sequence as depicted in Fig. 2.4 and can be viewed as a random process with a uniform probability distribution in the range $[-\Delta/2, \Delta/2]$ as shown in Fig. 2.5. Thus the power associated with the quantization error can be easily computed (ROSA, 2018):

$$\overline{e^2} = \sigma^2 = \int_{-\infty}^{\infty} e^2 PDF(e) de = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.7}$$

From (2.7) the peak Signal-to-Noise Ratio (SNR) at the output of an N-bit quantizer for a sinusoidal input can be obtained. The peak-to-peak amplitude of the sinusoid is $2^N\Delta$ and its power will be given by (2.8) (MALOBERTI, 2007):

$$P_{sin} = \frac{1}{T}\int_0^T \frac{X_{FS}^2}{4} sin^2(2\pi f t) dt = \frac{X_{FS}^2}{8} = \frac{(\Delta 2^N)^2}{8}. \tag{2.8}$$

From (2.8), the SNR of a N-bits ADC measured from an input sine wave is obtained by (2.9)

$$SNR = 10log\frac{P_{sin}}{P_{noise}} = 10log(2^N(12/8)) = 6.02N + 1.78\ dB. \tag{2.9}$$

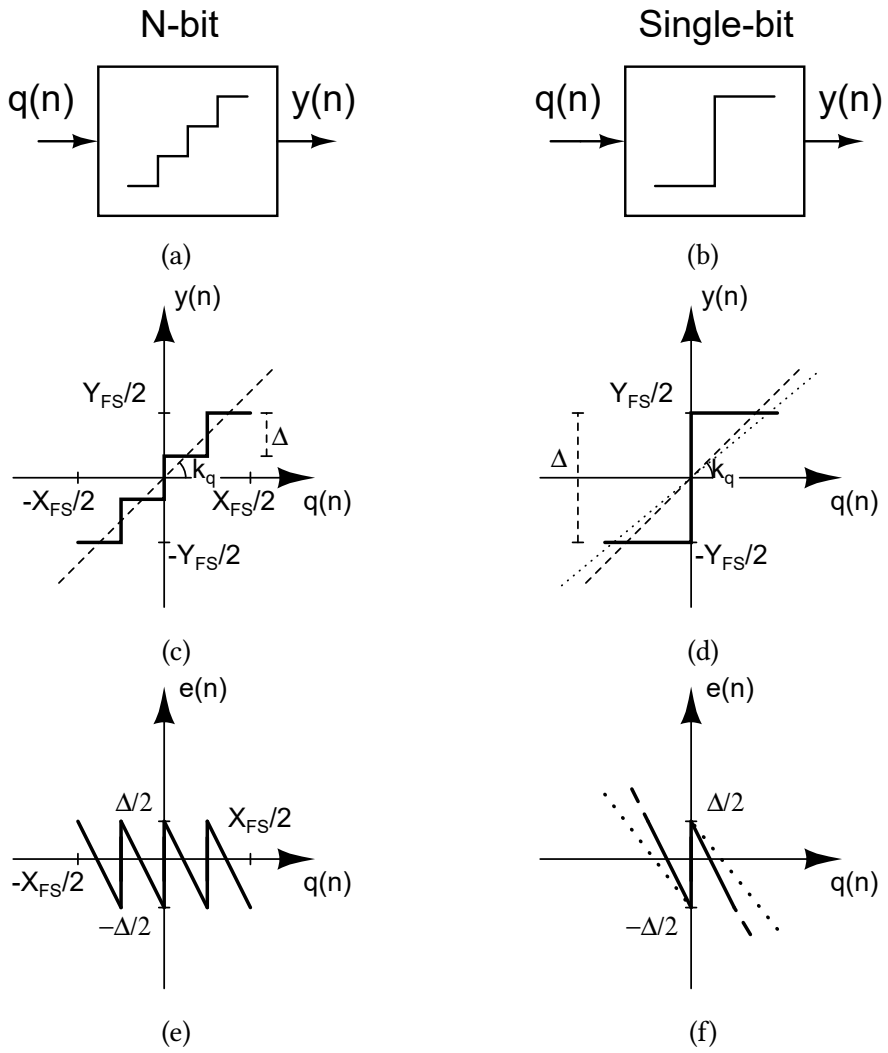


Figure 2.3: Quantization process: (a) Multi-bit quantizer block; (b) Single-bit quantizer block; (c) multi-bit quantization; (d) single-bit quantization; (e) multi-bit quantization error; (f) single-bit quantization error (ROSA, 2018).

Thus, the expected Effective Number of Bits (ENOB) of an ADC measured from an input sine wave will be given by (2.10)

$$ENOB = \frac{SNR - 1.78}{6.02}. \tag{2.10}$$

Meaning that for the increase in 6.02 dB in SNR, the ADC will effectively show 1 bit increase in resolution approximately.

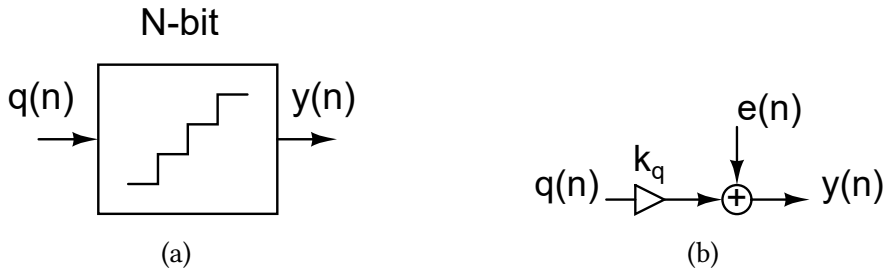


Figure 2.4: Equivalent quantizatizer linear model.

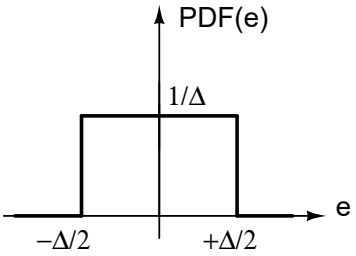


Figure 2.5: Quantization white noise Probability Density Function (PDF) (based on (ROSA, 2018)).

2.2 The ΣΔ ADC

The complete diagram of a ΣΔ ADC is shown in Fig. 2.6. The initial analog input is modulated by the ΣΔ Modulator as a pulse density in a sampling frequency much higher than the Nyquist rate, where the average of this pulses corresponds to initial input analog signal. To obtain the digital word, the oversampled signal must be filtered by a digital filter and its sample rate reduced by the decimator. This type of modulation allows for a phenomenon called "noise shaping" where the quantization error is amplified in the oversampled frequency, and suppressed on the signal band. Since the oversampling frequency is much higher than the Nyquist rate, the digital filter parameters are not demanding, simplifying its design.

This section will start with a more detailed explanation of the noise shaping, followed by the circuit realization of this phenomenon with a first order modulator and then, review several different types of implementation of ΣΔMs classified by the type of quantizer, the modulators order, cascaded modulators, band-pass modulators, discrete time and continuous time modulators, and the digital blocks of a ΣΔ ADC.

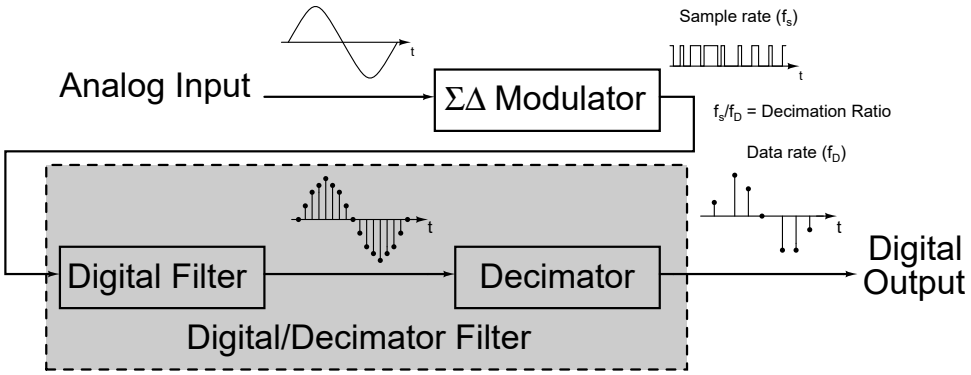


Figure 2.6: Complete ΣΔ ADC based on (BAKER, B., 2002).

2.2.1 Noise Shaping

Recalling to the discussion of quantization error in section 2.1.2, by oversampling the input signal, the SNR of the ADC is improved compared to what is described in equation (2.9) and is approximately (ROSA, 2018)

$$SNR \approx 6.02N + 1.78 + 10log_{10}(OSR). \tag{2.11}$$

To improve the ADCs performance even further, an operation known as noise shaping is performed and shows the biggest advantage of the ΣΔ modulation. This phenomena is obtained both through oversampling the input signal and by subtracting it from the output and then passing through a filter transfer function called the Noise Transfer Function (NTF). For low-pass ΣΔMs, the NTF must present a high-pass characteristic and is obtained from a differentiator filter with Z-domain transfer function given by (ROSA, 2018)

$$NTF = (1 - z^{-1})^L, \tag{2.12}$$

where L stands for the filter or shaping order. The noise shaping is depicted in Fig. 2.7 where the NTF is shown in red, separated from the original signal spectrum. The remaining quantization noise inside the original signal band is called the In-Band Noise (IBN).

From (2.12), considering $z = e^{j2\pi f/f_s}$ the NTF, if $f \ll f_s$ can be approximated to

$$|NTF(f)| = |1 - e^{j2\pi f/f_s}|^L = \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^L \approx \left(\frac{\pi f}{f_s}\right)^L \tag{2.13}$$

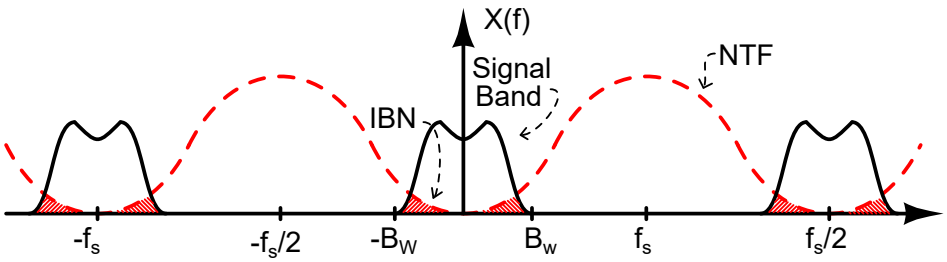


Figure 2.7: Spectrum of a ΣΔ modulated signal (adapted from (ROSA, 2018)).

and the IBN is

$$IBN = \int_{B_w}^{-B_w} S_E(f)|NTF(f)|^2 df \approx \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \tag{2.14}$$

Combining the obtained IBN with the SNR equation from (2.9), the SNR of a ΣΔ ADC is

$$SNR \approx 6.02N + 1.76 + 10log_{10}(\frac{2L+1}{\pi^{2L}}) + (2L+1)10log_{10}(OSR) \tag{2.15}$$

A noticeable improvement compared to equation (2.9). Now the SNR increases with the OSR by approximately 3(2L+1) dB/octave (ROSA, 2018).

First Order ΣΔ Modulator

The circuit realization of a first order DT-ΣΔ modulator is shown in Fig. 2.8. Fig. 2.8 also shows the ideal linear model of the same modulator replacing the quantizer and feedback DAC by a additive noise source E(z) and the integrator by

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{2.16}$$

From the linear model the system's transfer function can be easily be obtained:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{2.17}$$

Renaming and replacing z^{-1} by the Signal Transfer Function (STF) and $(1 - z^{-1})$ by NTF the equation becomes

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2.18}$$

meaning that the quantization error is multiplied by the NTF(z) which presents a high-pass characteristic, while the input signal is multiplied by the STF(z) which presents a low-pass

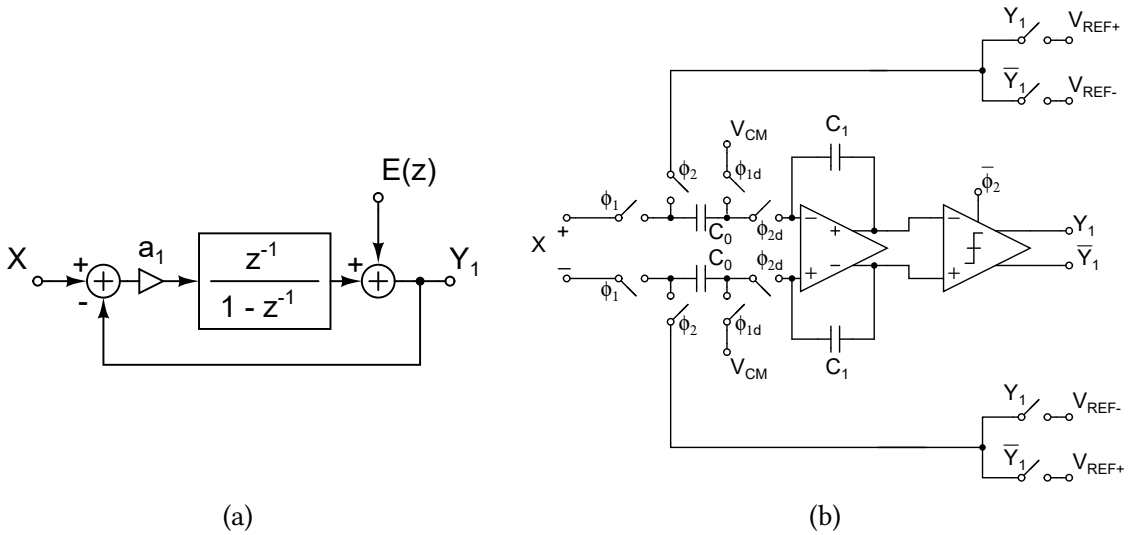


Figure 2.8: Realization of a first order ΣΔ modulator. (a) Linear model, (b) Circuit realization.

characteristic. The realization of a first order, single-bit ΣΔM is shown in Fig. 2.8 where the integrator function is performed by a switched-capacitor integrator, the single-bit ADC is a comparator and the feedback DAC is realized with two switches and two voltage references.

2.2.2 Classification of ΣΔMs

Multi-Bit Modulators

The SNR of a ΣΔM can be improved with the increase in the number of bits in the output quantizer. Fig. 2.7a and Fig. 2.7b show the diagram block of a multi-bit and single-bit quantizer respectively, and the transfer characteristics for each block are shown in Fig. 2.7c and Fig. 2.7d, while the quantization error is shown in Fig. 2.7e and Fig. 2.7f.

In more detail, the advantages of multi-bit quantizers are: 1)The in-band quantization noise power is reduced by approximately 6 dB per additional bit in the embedded quantizer, thanks to the smaller quantization step Δ, becoming essential in high-speed applications where impractical oversampling frequencies impose limited SNR, and are traded by the increase in the number of bit in the quantizer. 2) Internal non-linearities are weaker in multi-bit ΣΔMs than in their single-bit counterparts. The quantizer operation better fits the additive white noise model, and phenomena caused by nonlinear dynamics are less evident. 3) For a given order in the loop filter, the stability properties of multi-bit ΣΔMs are better than for single-bit ΣΔMs (ROSA, 2018).

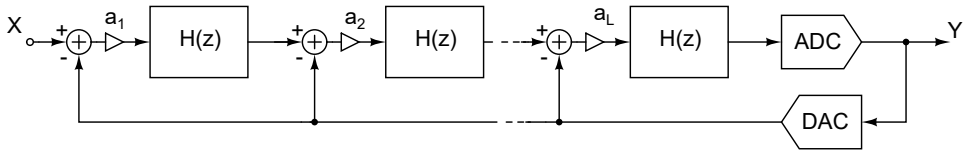


Figure 2.9: Higher order single loop ΣΔ modulator (ROSA, 2018).

The disadvantages of multi-bit quantizers are the increased complexity both in the feedforward ADC and the feedback DAC circuitry, also leading to non-linearities caused by device mismatching. Usually the resolution of multi-bit quantizers does not surpass 4-bits with few exceptions such as (STRAAYER; PERROTT, 2008) which presents a 5-bit Voltage Controlled Oscillator (VCO)-based quantizer, due to the high speed and high complexity required by these circuits.

High Order Modulators

Another way to improve a ΣΔM performance without altering its OSR is by increasing the noise shaping order as described by equation (2.15). The order of a modulator can be increased simply by adding integrators in series in the modulators feedback loop as shown in Fig. 2.9.

Ideally the NTF would be equal to (2.12), however in practice this is not possible as pure Finite Impulse Response (FIR) NTFs are prone to instability if L>2, exhibiting unbounded states (saturation) due to the high out-of-band gain of NTFs with order above 2. Usually, for higher order loops, the Infinite Impulse Response (IIR) NTFs are used in the form of $NTF(z) = (z - 1)^L/D(z)$, with D(z) being a polynomial defined by the modulators scaling coefficients. The approximate stability criterion for higher order noise shaping states that the gain of the NTF is (ROSA, 2018):

$$||NTF(z)||_\infty = max||NTF(z)|| \approx 1.5. \tag{2.19}$$

Although general stability conditions for modulators with order above 2 have not been defined, higher order ΣΔMs are conditionally stable with the proper selection of scaling coefficients (ROSA, 2018) and input amplitude (PAVAN; SCHREIER; TEMES, 2017), and have been widely adopted.

Cascade Modulators

Another way to achieve higher order noise shaping without the hindrance of complex stability criteria of single loop higher order modulator, is to cascade loops which present

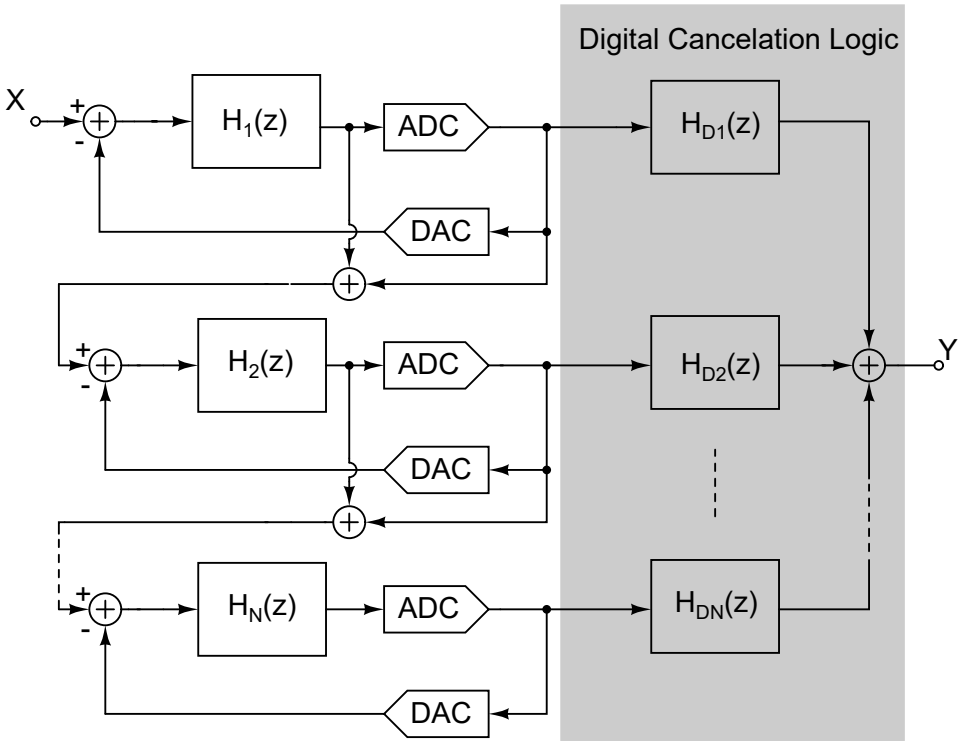


Figure 2.10: General topology of an N-stage cascade ΣΔM (ROSA, 2018).

general stability conditions, such as first and second order modulators. By cascading stable feedback loops, unconditionally stable higher order modulators can be obtained. These types of modulators are know as cascade modulators or Multi-Stage Noise Shaping (MASH) ΣΔ modulators.

Fig. 2.10 shows the general topology of a N-stage cascaded ΣΔM where each of the stages performs part of the quantization error modulation and passes to the next stage. The disadvantage of this implementation is that the cascading of the modulated signal does not result in a perfect higher order filter, therefore a Digital Cancellation Logic (DCL) must also be used to cancel inter-stage quantization error. This operation is performed in the digital domain as the output of each stage is already in a digital format.

For example a two stage cascade modulator would present the following transfer functions for the first and second stages respectively:

$$Y_1(z) = STF_1(z)X_1(z) + NTF_1(z)E_1(z) \tag{2.20}$$

$$Y_2(z) = STF_2(z)X_2(z) + NTF_2(z)E_2(z) \tag{2.21}$$

The overall output Y(z) is equal to:

$$Y(z) = H_1(z)Y_1 + H_2(z)Y_2, \tag{2.22}$$

choosing $H_1(z)$ and $H_2(z)$ as to cancel the first stage quantization error $E_1(z)$, $H_1(z) = STF_2(z)$ and $H_2(z) = +NTF_1(z)$, resulting in:

$$Y(z) = STF_1(z)STF_2(z)X(z) + NTF_1(z)NTF_2(z)E_2(z). \tag{2.23}$$

Assuming second order loop for both stages, $STF_1(z) = STF_2(z) = z^{-2}$ and $NTF_1(z) = NTF_2(z) = (1 - z^{-1})^2$, resulting in

$$Y(z) = z^{-4}X(z) + (1 - z^{-1})^4E_2(z). \tag{2.24}$$

Thus, achieving a 4^{th} order noise shaping with unconditional stability provided by the cascade of two second order loops (PAVAN; SCHREIER; TEMES, 2017). Limitations in this implementation come from the imperfections of the transfer functions, not perfectly canceling the error of previous stages. The nomenclature of this type of implementation describes each of the stages order, for example, 2-1 MASH ΣΔM (LONGO; COPELAND, 1988) stands for a second order loop followed by a first order loop, or 2-1-1 MASH ΣΔM (ORTMANNS; GERFERS; MANOLI, 2005) stands for a second order loop followed by two first order loops.

Band-Pass Modulators

The quantization noise can also be shaped as a band-pass filter as opposed to a high-pass filter described in the previous sections. This type of ΣΔ ADC is usually employed in the digitization of Intermediate Frequency (IF) or RF signals in wireless receivers due to its frequency selectivity, allowing for more modest requirements (PAVAN; SCHREIER; TEMES, 2017).

As depicted in Fig. 2.11, the IF or RF signal goes through the band-pass modulator where the quantization noise surrounds the desired signal spectrum, then a digital quadrature mixer shifts the signal band to DC, resulting both in the in-phase and quadrature components. Next the resulting signal goes through a digital low-pass filter and the decimation process occurs.

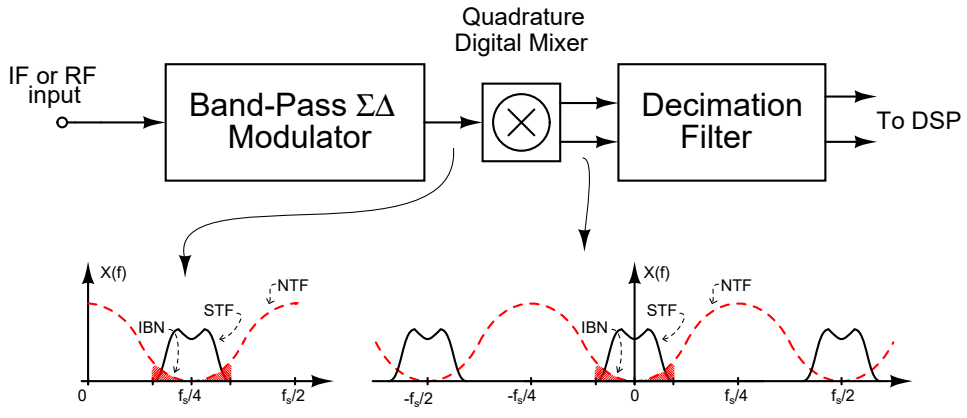


Figure 2.11: Band-pass ΣΔ ADC (PAVAN; SCHREIER; TEMES, 2017).

According to (PAVAN; SCHREIER; TEMES, 2017), the advantage of band-pass ΣΔM in wireless receivers, is that the first IF is digitized, reducing the complexity of a superheterodyne architecture to that of a direct conversion receiver without incurring the power and complexity penalties of adaptive digital processing.

Continuous Time Modulators

Continuous Time (CT) integrators can also be used in ΣΔM. CT-ΣΔM can achieve higher sampling rates with lower power consumption compared to equivalent Discrete Time (DT) ΣΔM (ROSA, 2018) and for this reason have become more common in state-of-the-art high speed ΣΔMs. In general DT modulators are more common in high precision ΣΔ ADCs where a high resolution is required.

The most significant difference between DT and CT is the location of the sampling operation, depicted in Fig. 2.12, where for DT modulators it occurs at the input of the system, performed by S&H circuit, whereas for CT modulators it is performed before the quantization operation, allowing for CT integrators to be used.

Fig. 2.8 shows the circuit implementation of a first order CT-ΣΔM. Compared to the its DT counterpart of Fig. 2.8, the only difference is the use of a CT integrator. Combined with the amount of DT-ΣΔMs reported in the literature compared to CT-ΣΔMs and the relative simplicity in the changes from DT to CT modulators, transformations from the Z-domain to S-domain have been developed for designing CT-ΣΔMs starting from the DT loop filter (ORTMANNS; GERFERS, 2006).

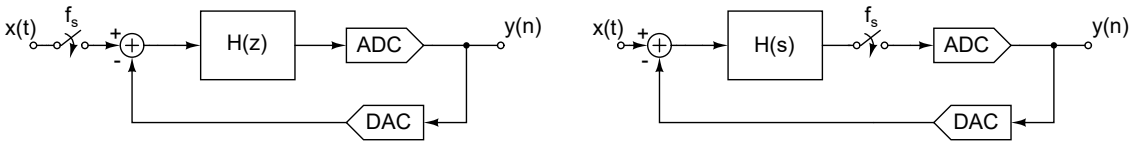


Figure 2.12: Comparison between (a) DT modulator; (b) CT modulator (ROSA, 2018).

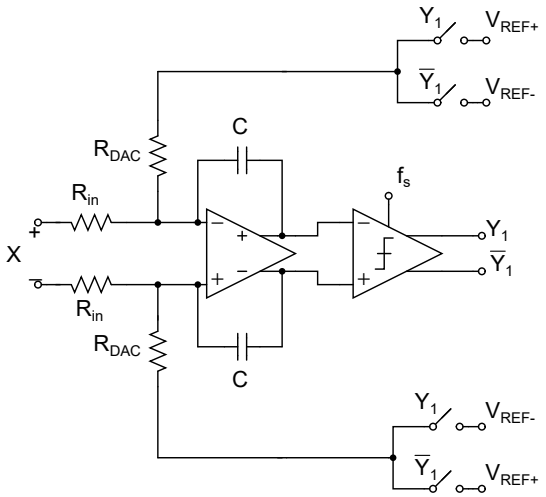


Figure 2.13: Example of implementation of a continuous time ΣΔM.

2.2.3 Digital Blocks of the ΣΔ ADC

For a complete ADC a decimation filter is required, as depicted in the complete ADC scheme of Fig. 2.6. The output of the modulator, although, already a digital signal, presents an oversampled waveform containing both the original signal band, and the noise shaped quantization error. To remove the quantization error, a low-pass filter (for high-pass noise shaping) is required, and to reduce the output data rate down to the Nyquist rate, a decimation operation must be performed.

These operations (filtering and decimation) are implemented in the same digital block, by Cascade-Integrator-Comb (CIC) structures shown in Fig. 2.14, only requiring digital delays and adders. The Z-domain transfer function of the CIC structures is given by

$$H_{CIC}(z) = \frac{1 - z^{-M}}{1 - z^{-1}}. \tag{2.25}$$

This transfer function is also known as the SINC filter

$$SINC_M^k(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}} \right)^k, \tag{2.26}$$

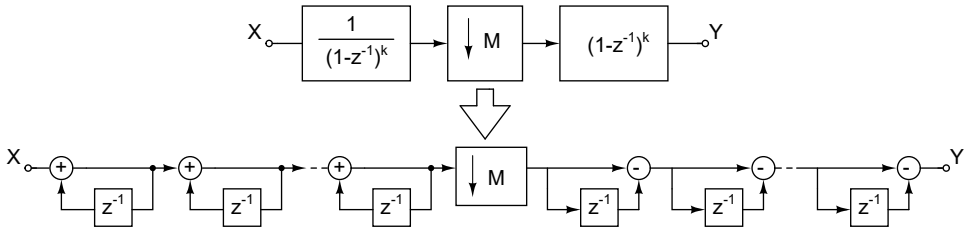


Figure 2.14: Block diagram of a k-order ($sinc^k$) CIC decimation filter (ROSA, 2018).

where M is the decimation factor and k is the order of the filter. (PAVAN; SCHREIER; TEMES, 2017).

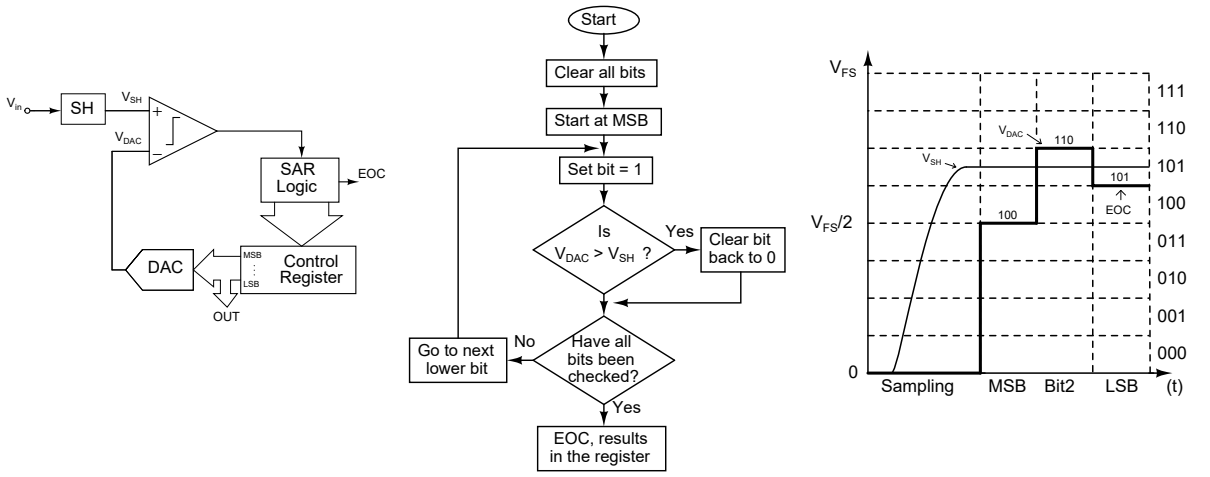
2.3 Other Popular AD Conversion Techniques

In this section, a few of the main topologies and techniques being used today in state-of-the-art non-ΣΔ ADCs will be reviewed, describing its basic operation, highlighting its advantages and challenges during the design. Due to the context of this works, examples of reconfigurability in different topologies will also be highlighted.

2.3.1 Successive Approximation Register

The Successive Approximation Register (SAR) ADC is by far the most popular topology for Analog-to-Digital conversion. Its operation is very simple, basically performing a binary search though all quantization levels successively until it reaches its final digital answer (BAKER, R. J., 2010). In detail, its operation based on Fig.2.15a is: first the analog input V_{in} is sampled by a sample and hold circuit. At the first sample the voltage V_{SH} will be compared with the result of the conversion of the Most Significant Bit (MSB) by the DAC V_{DAC}. If V_{DAC}>V_{SH} the SAR logic will register this bit as 1 and select the next MSB. If V_{DAC}<V_{SH} the logic will register the bit as 0. The process is repeated with the next MSB until all bits are checked. Then an End of Conversion (EOC) bit will flag 1, indicating the end of conversion. The flowchart of the SAR operation is described in Fig. 2.15b (J.TOCCI; WIDMER; MOSS, 2007). The waveform of a 3-bit SAR ADC is depicted in Fig. 2.15c where an analog input between $6V_{FS}/8$ and $5V_{FS}/8$ is converted. Each step of the conversion increases the precision of the comparison totaling $(N + 1)$×clock cycles as the total conversion time.

Due to its reliance on high precision and high speed of comparison, the design bottleneck of this topology relies on the accuracy of the analog circuitry containing the S&H



(a) (b) (c)

Figure 2.15: Successive approximation register ADC. (a) Diagram, (b) flowchart (J.TOCCI; WIDMER; MOSS, 2007), (c) conversion waveform (MALOBERTI, 2007).

(non-linearity), comparator (offset, hysteresis and comparison time) and DAC (mismatch). SAR ADCs often require complex bootstrapping circuits for the S&H switches, and calibration techniques for both the comparator and the DAC. The accuracy requirements also affect the layout implementation, demanding careful matching of the analog components.

The SAR topology is the most versatile topology achieving both high resolutions and high speeds with relatively simple design, reaching up to 18 bits of resolution in lower sampling rates (HUMMERSTON; HURRELL, 2017) and sample rates in the scale of GHz with lower resolutions (7 bits) (RAMKAJ et al., 2018) without the use of time-interleaved techniques. For this reason the SAR ADC is the most popular topology for applications in any frequency range that require resolutions below 20 bits.

Examples of Reconfigurability

There are few reported works on reconfigurability in SAR ADCs. An example is found in (LIU et al., 2021) where the ADC trades 1 bit of resolution to double its data rate, where one mode presents 60 MS/s with 9 bits resolution mode and another mode with 120 MS/s with 8 bits resolution. Another interesting example is found in (SHEN et al., 2018) where a SAR topology varying the resolution from 10 to 12 bits and the sampling rate from 20 to 80 MS/s. However the bandwidth variation is achieved through the time-interleaving technique, which can be employed in other ADC topologies as well. Other works such as (HU et al., 2019) and (YIP; CHANDRAKASAN, 2013) propose reconfigurability only through the

resolution variation, not varying the output data rate. Another solution found in (TANG et al., 2021) employs a pipelined SAR topology to achieve 0.4 to 40 MS/s with linear power consumption scaling with 12.3 bits of resolution.

2.3.2 Pipeline

The pipeline converter uses a cascade of conversion stages where each of this stages performs the low-resolution conversion of a fraction of the total number of bits of the complete ADC. Fig. 2.16 (CHIU; GRAY; NIKOLIC, 2004) shows the diagram of a k-Stages Pipeline ADC where each stage converts two bits and the total number of bits is defined by $n_1 + n_2 + ... + n_k$.

The basic operation of each stage is also highlighted in Fig. 2.16 where the input voltage V_1 is subtracted from the Analog-to-Digital-to-Analog conversion of the same signal. The result of this operation is passed to the subsequent stage, amplified by the residue amplifier to the full-scale range of the ADC. This is important because it allows the sharing of and identical reference throughout the pipeline stages. This reliance on the amplification in each stage also relaxes the impact of circuit non-idealities such as noise, non-linearity and offset, in the later stages of the pipeline (CHIU; GRAY; NIKOLIC, 2004). The timing diagram of Fig. 2.17 taken from (MALOBERTI, 2007) shows the sequential control of a 10-bit, 5 stages, 2-bit per stage pipeline ADC. The analog input is sampled at the t-th clock cycle, the first stage converts bits b_9 and b_8 at the (t+1)-th clock cycle, bits b_7 and b_6 are converted at the next clock cycle and so on, until the 10 bit conversion of the initial analog input signal is achieved at the (t+6)-th clock cycle. The total conversion time is dependent on the total number stages.

The conversion accuracy of Pipeline ADCs depend on the precision of the residual signal, thus mismatch on the D/A conversion components, offset of comparators and amplifiers are the main limiting factors in pipeline ADC resolution. Also for the conversion speed the settling time of the residue amplifiers are the main limiting factors (CHIU; GRAY; NIKOLIC, 2004).

Examples of Reconfigurability

Reconfigurability in Pipeline ADCs are more common when compared to SAR topologies. A recent example is (HERSHBERG et al., 2020) where the Pipeline ADC maintains its 11 bit target with a SNR of 59.8 across a sampling frequency range varying from 1MS/s up to 1GS/s. In this example, however, the power consumption does not scale with sampling frequency variation, staying at 10.9 mW for every frequency.

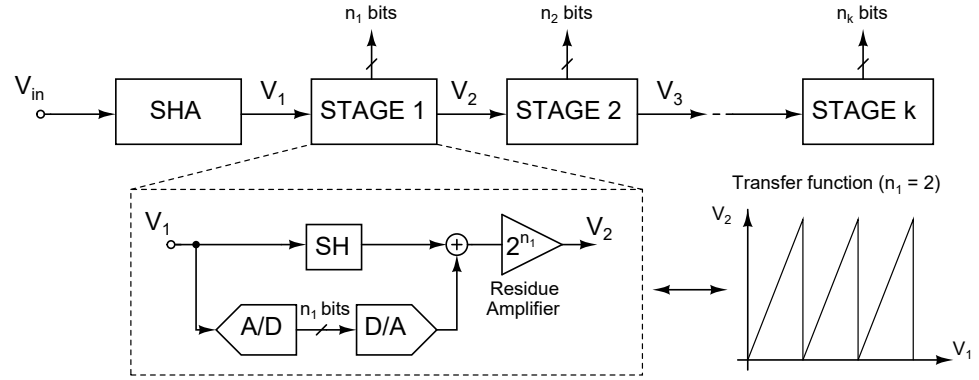


Figure 2.16: 2-bits per stage Pipeline ADC diagram (CHIU; GRAY; NIKOLIC, 2004).

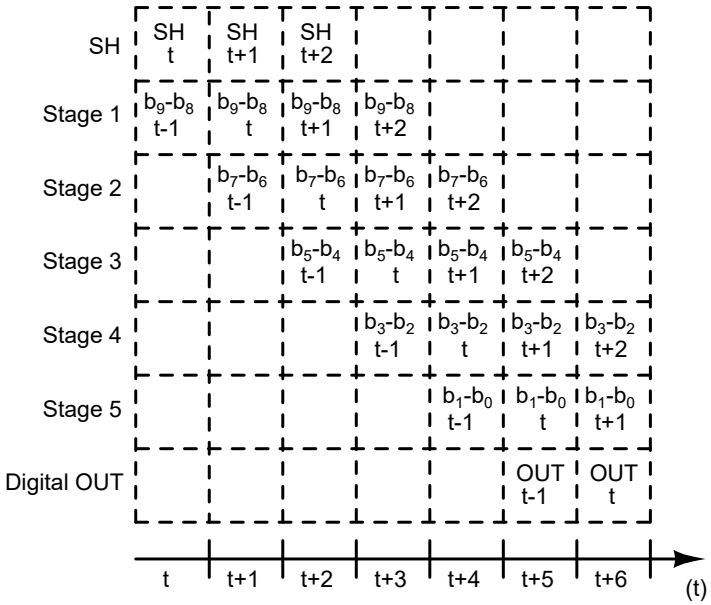


Figure 2.17: Pipeline timing diagram (MALOBERTI, 2007).

2.3.3 Time-Interleaving

Time-Interleaving is technique applied to ADCs to increase the conversion speed by using a number of parallel slower speed ADCs simultaneously. The architecture is shown in Fig 2.18. The input is sampled at a frequency f_s higher than what the individual ADCs are capable of converting. The analog demultiplexer distributes the input signal to each parallel ADCs, and the digital multiplexer sequentially selects the output of each channel to obtain the full speed digital word (MALOBERTI, 2007). The maximum conversion rate is dependent on the number of parallel ADCs.

This technique is becoming ubiquitous in state-of-the-art ultra high speed ADCs due to the challenges of reaching high speeds in traditional topologies such as SAR, Pipeline and $\Sigma\Delta$. The technique is often used to multiply the output data rate achieving speeds in the magnitude

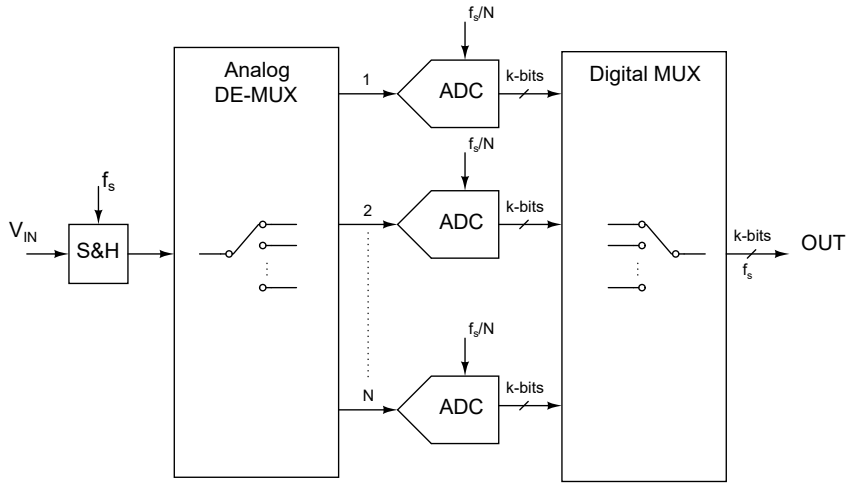


Figure 2.18: Time-Interleaved architecture diagram (MALOBERTI, 2007).

of tens of Giga Samples per Second (GS/s). An example is (XU; ZHOU; CHIU, 2017) where 24 GS/s is achieved with 6 bit resolution using time-interleaving with SAR ADCs with 23 mW of power consumption. (SUN et al., 2019) achieves 56 GS/s with 8 bits with 702 mW of power consumption also using SAR ADCs. An example of Pipeline ADCs being used with time-interleaving is found in (WANG, X. et al., 2019) where 14 bits of resolution with 500 MS/s are obtained. Now for ΣΔ ADCs, (DAYANIK; WEYER; FLYNN, 2017) shows an ADC achieving 5 GS/s with 11 bits of resolution and 233 mW of power comsumption.

Examples of Reconfigurability

Reconfigurability becomes an obvious opportunity for time-interleaved ADCs due to its parallel nature. The work in (DANESH et al., 2011) shows a reconfigurable ADC employing the time-interleaved technique to achieve 1GSps 7-bit, 500MSps 8-bit, and 250MSps 9-bit with 400 fJ/step for each configuration. (HSU et al., 2007) presents a pipeline ADC using time-interleaving to achieve reconfigurability with 1.1 GS/s with 7 bits, 550 MS/s with 7 bits and 550 MS/s with 5 bits with a power consumption of 46 mW, 30 mW and 13 mW respectively.

2.4 Recent Trends in ADC Design

In regards to the recent trends in state-of-the-art Analog-to-Digital Converters, a review of publications in the Journal of Solid State Circuits from January of 2018 to December 2021 was carried out, totaling 48 issues. Fig. 2.19 shows the results. In total 95 ADC papers were

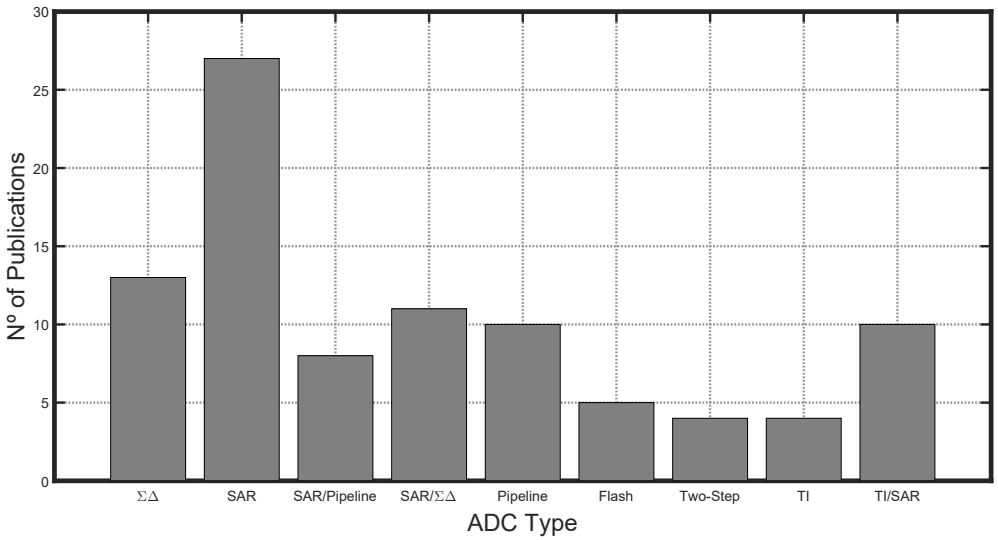


Figure 2.19: Compilation of papers related to ADCs published in the *Journal of Solid State Circuits* since 2018.

published, with a notorious advantage to projects that employ SAR type ADCs. A very interesting trend is the use of topologies that use two or three techniques, for example, the use of SAR with noise shaping (ΣΔ modulation), or SAR and Pipeline, and even examples of Pipelined ADCs that employ SAR with noise shaping. Overall, the ΣΔ topology still is very popular, ranking in second, and the noise shaping technique is very popular in SAR ADCs. A few examples of techniques that only appeared once or twice (for example ramp ADC and a Δ modulation ADC) were not included in the graph.

ΣΔ ADCs, due to its necessity of an oversampling frequency much larger than Nyquist, are not the best alternative for applications that require high frequency (e.g. hundreds of MHz to GHz) as shown by Fig. 2.20 from (MURMANN, 2022) where a survey of all reported ADCs in the International Solid-States Circuits Conference (ISSCC) and the IEEE Symposium on VLSI Technology and Circuits are documented since 1997. Generally the ΣΔ topology is dominant in low frequency applications such as audio devices, CMOS camera sensors and instrumentation, where high precision is more important. Nevertheless, this type of ADC is still viable for wireless receivers up to 4G standards (e.g. LTE-A with 20 MHz bandwidth), as shown by (BETTINI et al., 2015), (LI et al., 2013) e (CROMBEZ et al., 2010). To obtain even higher frequencies in reconfigurable ADCs, innovations employing hybrid topologies have been reported in (JIE; ZHENG; FLYNN, 2012) and (TAO; RUSU, 2015) combining ΣΔ with Pipeline, SAR with noise shapping in (JIE; ZHENG; FLYNN, 2019) and (SONG et al., 2020), and of course time-interleaving using ΣΔ ADCs in (DAYANIK; WEYER; FLYNN, 2017).

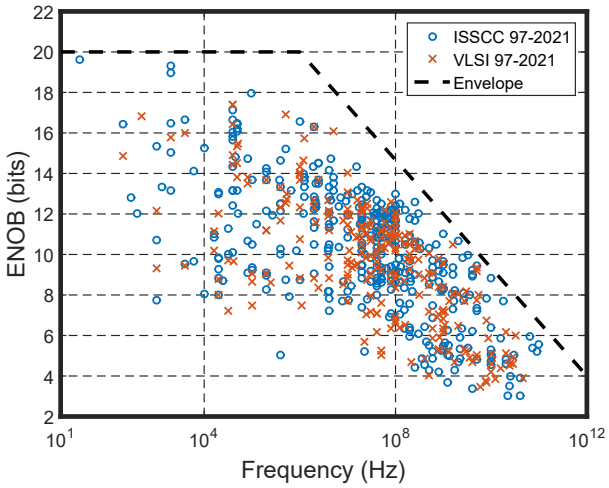


Figure 2.20: State-of-the-art ADCs in relation to resolution versus bandwidth from (MURMANN, 2022).

2.5 Main Bibliography for the Project

The most popular reference about ΣΔ converters theory is (PAVAN; SCHREIER; TEMES, 2017), and will be widely used for theory review in this project. The book (ROSA, 2018), presents a very practical focus in ΣΔ modulator development, in addition to a more up to date review of ΣΔ modulation theory, and will also be widely used in this work. The book (MORGADO; RIO; ROSA, 2011) presents a compilation of reconfigurable ΣΔ modulators for multi-standard wireless applications, and was the inspiration for this project.

For the clock synthesizer design the book (RAZAVI, 2020) will be the main reference. This book, published in 2021, presents an extremely detailed phase-locked loop theory, highlighting each PLL sub-circuit with practical state-of-the-art examples.

For the auxiliary building blocks of each system (ΣΔM and PLL), the book (RAZAVI, 2017) will be the main reference, presenting the broadest and most detailed information relating to analog CMOS circuit design.

Chapter 3

Circuit Design

3.1 Methodology

In large SoC, designs the modeling of a system in higher and more abstract levels is essential as analog and mixed-signal designs become larger and more complex. High level generalized simulation tools such as SIMULINK (MATLAB, 2021) provide a good understanding of the architecture to be developed, however as the project approaches the physical implementation, integration between transistor level sub-circuits and macro-model sub-circuits is essential for system debugging, therefore a more specialized modeling tool becomes indispensable.

In complex analog integrated circuits, the most common approach to design is the *top-down bottom-up* hierarchical synthesis methodology (ROSA, 2018). In this methodology, after the the system specifications are defined, behavioral simulation with non-ideal components in high level simulators, such as SIMULINK, are performed to evaluate the feasibility of the architecture. Next, simulations with macro-models are performed in the same simulation tool of the transistor level implementation.

For this project both the macro-model and transistor level simulations were performed with SPECTRE (CADENCE DESIGN SYSTEMS, 2020) using Verilog-A models, in the Cadence Virtuoso Analog Design Environment. Then, after the validation with macro-models, the transistor level implementation starts with each sub-circuit. This step of integration with transistors and macro-models is of extreme importance because simulations tend to consume an impractical amount of time in the latter stages of development. Finally, after transistor level validation, the physical implementation of the circuit starts, encompassing the layout implementation, extracted layout simulations and fabricated chip measurement.

In this type of methodology, on every hierarchical level, the return to previous levels can take place if the defined requirements at the current level are not met. Ideally, well though out and carefully planned specifications will avoid architectural rework, and thus reduce the total project time. This approach is essential for the analog integrated circuit design workflow due to impractical simulation times during transistor level implementation and post-layout simulations of complex systems, rendering circuit debugging unfeasible in the expected time-frame of the market competitive integrated circuits industry.

In this work the *top-down bottom-up* methodology was used both in the development of the ΣΔ modulator and the clock synthesizer. Throughout this chapter, all major sub-circuits will be highlighted with its macro-model in Verilog-A and transistor-level circuit implementation. Although simulations in SIMULINK were performed for the ΣΔM using two different toolboxes ((RUIZ-AMAYA et al., 2005) and (FORNASARI; MALCOVATI; MALOBERTI, 2005)) they will not be highlighted due to the simplicity of the simulations performed and for the sake of brevity of this work.

3.2 Multi-Standard Receiver Considerations

The proposed modulator will operate in GSM (EDGE), Bluetooth and UMTS (W-CDMA) standards, and the respective bandwidths are presented in table 3.1. The requirements of each operation mode depends on Dynamic Range (DR), gain, linearity and noise specifications of the sub-circuits in the receiver front-end (antenna, Low-Noise Amplifier (LNA), local-oscillator and mixer) and specially the BB filter selectivity. According to (BETTINI et al., 2015) the DR requirements of a multi-standard ADC depend on the SNR necessary to achieve the desired Error Vector Magnitude (EVM), on the Peak-to-Average-Power Ratio (PAR) of the modulated signal, and on the residual interferers not filtered by the preceding BB filter.

Exemplified by Fig. 3.2 (BETTINI et al., 2015) in the blocker template for Long Term Evolution (LTE), the requirements for the ADC DR, including also a headroom for non-idealities and the Programmable Gain Control (PGC) gain step. The BB filter selectivity will affect the range of residual blocker range to be accommodated in the ADC required DR. Fig. 3.3 presents the required ADC DR based on the BB filter cut-off frequency for the GSM standard, also taken from (BETTINI et al., 2015). Depending on the BB filter selectivity the

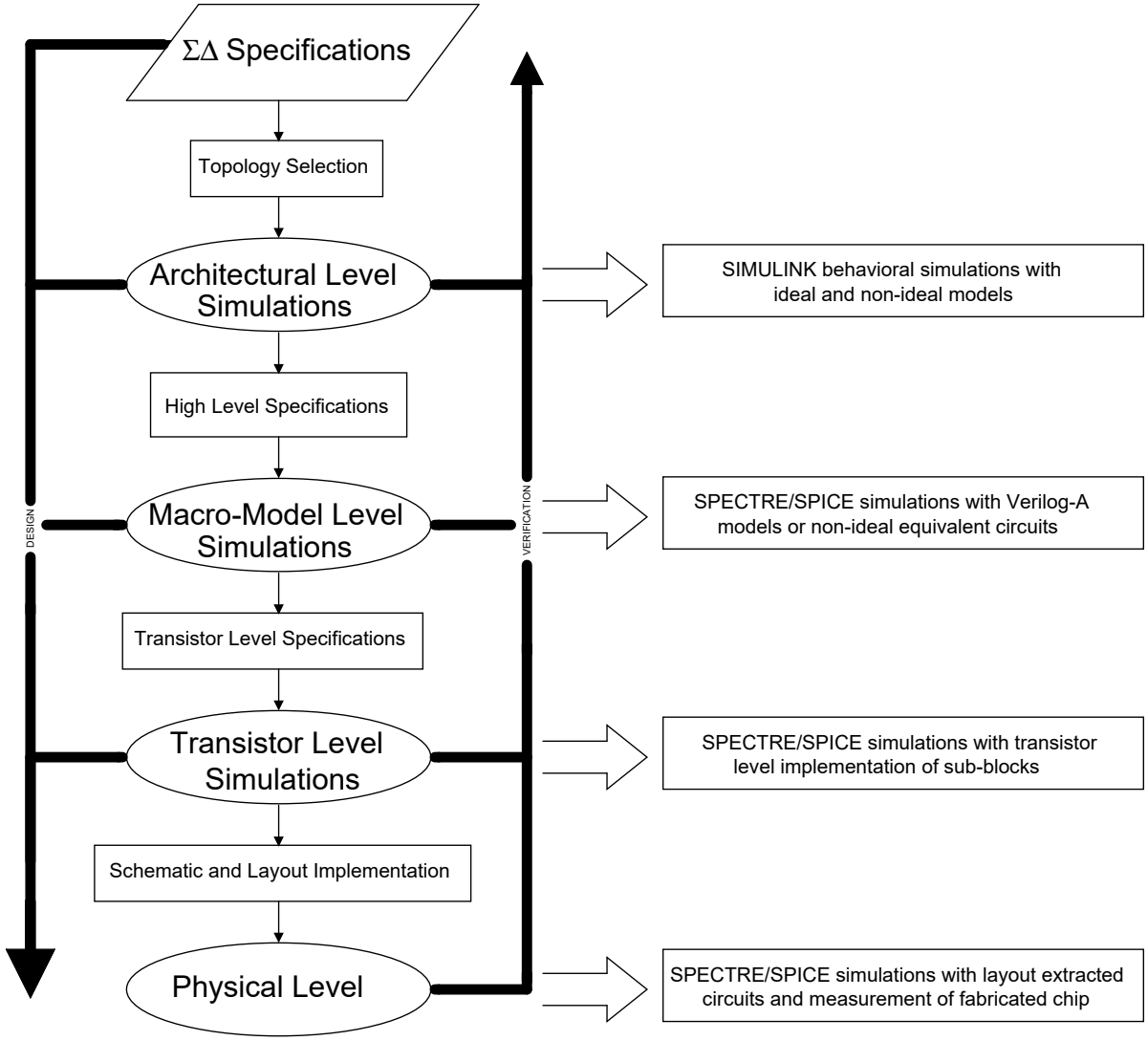


Figure 3.1: Top-down/bottom-up methodology (adapted from (ROSA, 2018)).

required DR can vary from 54 dB up to 85 dB, considering the close relationship between SNR and DR, 30 dB in SNR is equivalent to approximately 5 bits. The drawback of filters with high selectivity is its complexity of implementation (e.g. higher order filters).

The receiver planning is out of the scope of the work, for this reason the DR and SNR requirements for GSM, Bluetooth and UMTS were based on other multi-standard reconfigurable ΣΔ modulators (MORGADO; DEL RÍO, et al., 2010), (MORGADO; RIO; ROSA, 2011), (BETTINI et al., 2015), (KE et al., 2010), (CROMBEZ et al., 2010). For GSM the target SNR is 74 dB (12 bits), Bluetooth is 68 dB (11 bits) and UMTS is 50 dB (8 bits), summarized in table 3.1.

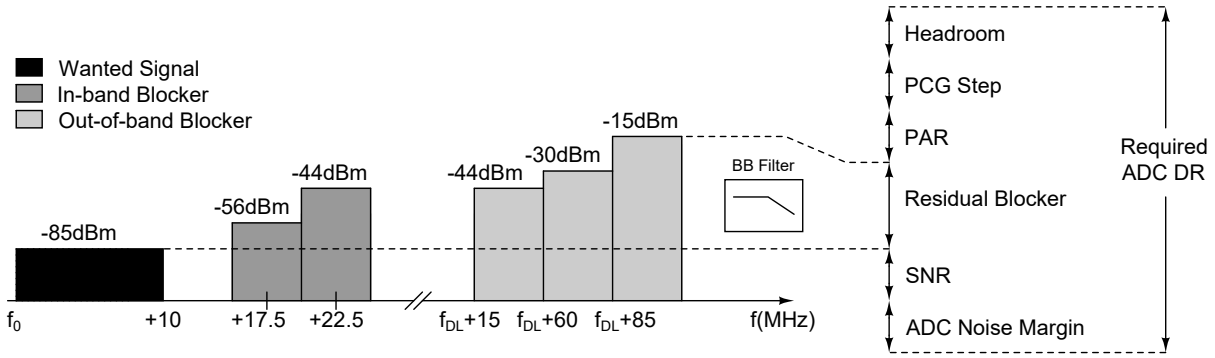


Figure 3.2: Blocker template for LTE mode (BW = 10 MHz), and corresponding required ADC DR (f_{DL} represents the higher end of the downlink operation) (BETTINI et al., 2015).

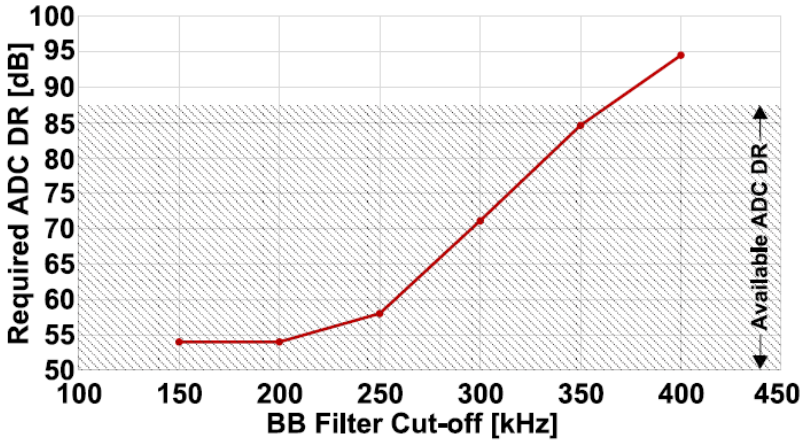


Figure 3.3: Required ADC DR versus BB filter cut-off in EDGE mode (Alternate channel test:f_{bl} = 0.4 MHz , P_{bl}/P_{ws} = 41 dB) (BETTINI et al., 2015).

Table 3.1: Requirements for the ΣΔM in each operation mode.

Parameter/Mode	GSM	BT	UMTS
Resolution (bits)	12	11	8
SNR (dB)	74	68	50
Bandwidth (MHz)	0.2	0.5	2

3.3 Reconfigurable ΣΔ Modulator

Fig. 3.4 shows the block diagram of the complete system. To achieve the target ENOB for GSM, the modulator will operate in a 2^{nd} order configuration with an oversampling frequency of 40 MHz enabling only two integrators and a single bit quantizer, based on (3.1) (MALOBERTI, 2007) where M is the number of bits in the quantizer, the maximum achievable SNR is around

88 dB which is more than enough to reach the requirements.

$$SNR = 10log_{10}\frac{15M^2OSR^5}{2\pi^4} \tag{3.1}$$

For Bluetooth operation, the multi-bit quantizer is enabled, disabling the single bit one, while the oversampling frequency goes up to 60 MHz. From (3.1) these parameters are more than enough to reach the requirements of table 3.1. Finally, for the UMTS mode, all the circuit is enabled, the multi-bit quantizer is connected to the second stage output, the oversampling frequency is raised to 80 MHz and the DCL is enabled. SIMULINK simulations with non-ideal circuits were performed to evaluate if this topology meets the requirements for this particular mode of operation.

Although several stable 3rd and 4th order modulators have been reported in the literature, their stability criteria are not as well defined as 1st and 2nd order modulators ((ROSA, 2018), (PAVAN; SCHREIER; TEMES, 2017)). A solution to achieve higher order noise shaping with stability, is to cascade 2nd and 1st order stages. However, only cascading the stages is not enough, as the first stage quantization error remains in the transfer function, thus a DCL circuit must be used.

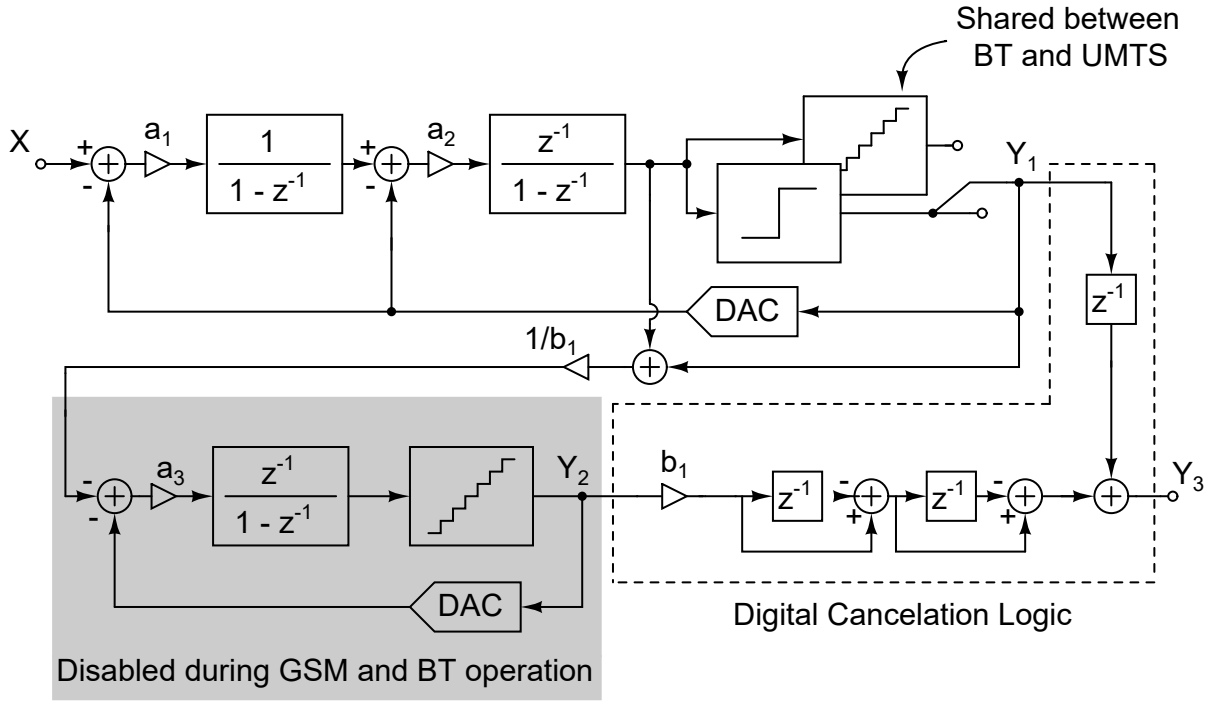


Figure 3.4: Proposed reconfigurable ΣΔ Modulator block diagram.

From Fig. 3.4 the transfer function for UMTS can be inferred. From the block diagram, adjusting the gains a_1, a_2, a_3, b_1 and considering both stage quantizers as error sources $E_n(z)$ in (3.2) and (3.3), (3.4) is obtained, and the NTF and STF can be defined, as represented by (3.5) (LONGO; COPELAND, 1988).

$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})^2 E_1(z) \tag{3.2}$$

$$Y_2(z) = -z^{-1}E_1(z) + (1 - z^{-1})E_2(z). \tag{3.3}$$

Following $Y_1(z)$ and $Y_2(z)$ signal paths and applying the DCL:

$$Y_3(z) = z^{-2}X(z) + (1 - z^{-1})^3 E_2(z) \tag{3.4}$$

where $E_1(z)$ and $E_2(z)$ are the first and second stages quantization errors. Rewriting:

$$Y(z) = X(z)STF(z) + E_2(z)NTF(z). \tag{3.5}$$

The NTF(z) and STF(z) from (3.5) present the biggest advantage of ΣΔ Modulation called noise-shaping, where the NTF(z) has a high pass characteristic, attenuating the noise inside the band of interest, while amplifying it outside the band of interest. The STF(z) presents a low-pass filter characteristic, thus preserving the original signal.

For the GSM and BT operations a large portion of the circuit is turned off (from Fig. 3.4 the second stage, highlighted in gray, and the DCL), therefore, the transfer function is much simpler to obtain, and is given by (3.6):

$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})^2 E_1(z), \tag{3.6}$$

or, alternatively

$$Y_1(z) = X(z)STF(z) + E_1(z)NTF(z). \tag{3.7}$$

Gains a_1, a_2, a_3 and b_1 are optimized for the 2-1 MASH topology based on (MARQUES et al., 1998) which presents a optimization study in several ΣΔ topologies, and optimization via macro-modeling simulations. The values are: $a_1 = 1/4$; $a_2 = 1$; $a_3 = 1$; $b_1 = 4$.

The realization of the ΣΔM in circuit form is presented in Fig. 3.5. The operation modes are chosen by the SEL bit that controls the duplexers wich in turn, control the signal path.

During GSM and Bluetooth operations, the second stage amplifier is disabled (part of the circuit highlighted in gray). Clock phases ϕ_1 and ϕ_2 are non-overlapping and ϕ_{1d} and ϕ_{2d} are their delayed versions. The voltage references V_{REF+} and V_{REF-} are taken from ideal voltage sources, and are set as 1.4 V and 400 mV for all modes of operation.

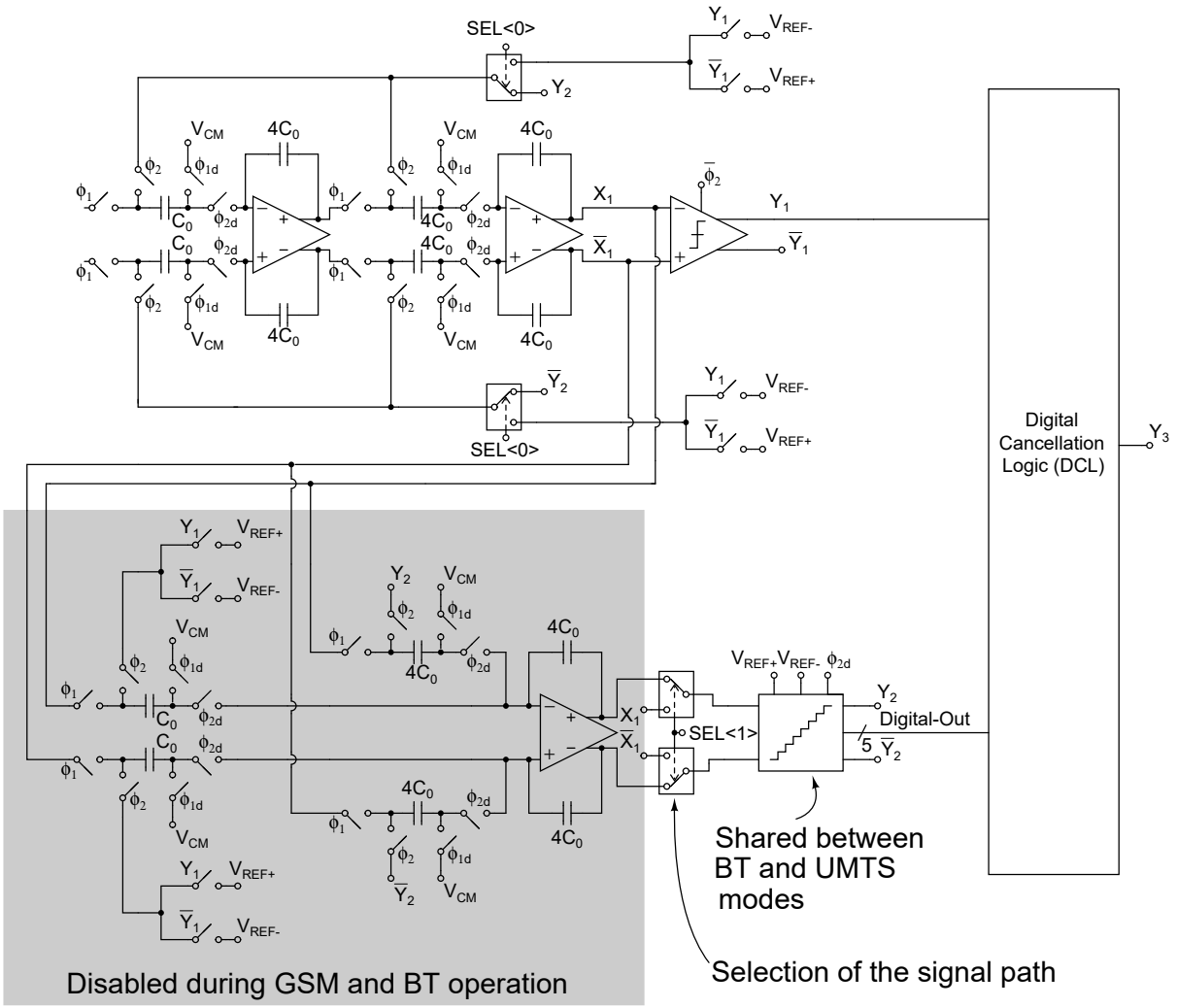


Figure 3.5: Circuit implementation of the reconfigurable ΣΔ Modulator.

3.3.1 Operational Transconductance Amplifier

In most ΣΔM, the Operational Transconductance Amplifier (OTA) is the most critical sub-circuit for SNR degradation. In particular, the main error sources are dominated by three characteristics: Finite Gain-Bandwidth (GBW), finite Slew-Rate (SR) and finite DC open loop gain. Usually, in DT modulators, a gain of 50 dB, a GBW of 4 times the oversampling frequency and a SR of 5 times the oversampling frequency are a good starting point for the design (ROSA, 2018).

Since the beginning of this project, a lot of though was put in the planning of the OTA requirements. From the review of similar ΣΔM topologies, and high-level simulations with non-idealities, its requirements were defined as shown in table 3.2.

Table 3.2: Requirements for the OTA in each operation mode.

Parameter/Mode	GSM	BT	UMTS
Gain (dB)	50	50	50
Gain Bandwidth (MHz)	300	400	500
Slew-Rate (V/µs)	300	500	750

Macro-Modeling

Verilog-A was built with the aim of becoming an analog circuit language descriptor, thus it is always desirable to work with simple equivalent circuits of complex systems. For the operational amplifier, the equivalent model from Fig. 3.6 is used (WANG, Y.; WANG, Y.; HE, 2008). From this model the amplifier's main specifications can be inferred:

$$GBW = \frac{g_m}{2\pi C_g} \tag{3.8}$$

$$SR = \frac{I_{out}}{C_g} \tag{3.9}$$

$$Gain = R_g g_m \tag{3.10}$$

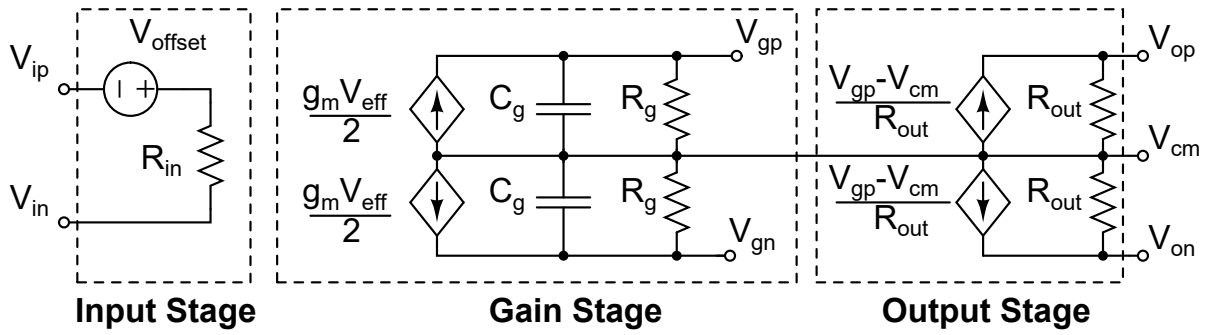


Figure 3.6: Equivalent circuit of the operational amplifier for the Macro-Model.

Then, from the model of Fig. 3.6 the circuit can be described in Verilog-A highlighted in the code snippet 3.1. Initially the input stage effective voltage is inferred. Next, for the gain

stage each node current is described. Finally the same process is repeated for the output stage. Thus, by previously defining in the code the values of g_m, R_g, C_g and R_{out} all the main OTA specifications from 3.8 to 3.10 can be set.

Listing 3.1: Snippet of the Operational Amplifier code in Verilog-A.

```
analog begin
  //Input Stage
  vin_eff = V(IN_P,IN_N) - vin_offset;
  //Reference Voltage Definition
  V(vref_aux) <+ V(VREF);
  I(IN_P,IN_N) <+ vin_eff/rin;
  //Gain Stage
  I(vref_aux, outp_aux) <+ (gm/2)*vin_eff;
  I(vref_aux, outn_aux) <+ -(gm/2)*vin_eff;
  I(outp_aux, vref_aux) <+ Cg*ddt(V(outp_aux,vref_aux));
  I(outp_aux, vref_aux) <+ V(outp_aux, vref_aux)/Rg;
  I(outn_aux, vref_aux) <+ Cg*ddt(V(outn_aux, vref_aux));
  I(outn_aux, vref_aux) <+ V(outn_aux, vref_aux)/Rg;
  //Output Stage
  I(vref_aux, OUT_P) <+ (V(outp_aux) - V(vref_aux))/rout;
  I(OUT_P, vref_aux) <+ V(OUT_P, vref_aux)/rout;
  I(vref_aux, OUT_N) <+ (V(outn_aux) - V(vref_aux))/rout;
  I(OUT_N, vref_aux) <+ V(OUT_N, vref_aux)/rout;
end;
```

Transistor Implementation

The topology used for the OTA consists of a modified folded-cascode topology, with a cross-coupled input pair to improve gain as proposed by (MEZYAD M. AMOURAH, 2001). The topology is shown in Fig. 3.7. Due to the small available supply voltage, and the need of high gain and high speed of operation required for the modulator, a positive feedback gain enhancement technique was used in the amplifier design, as to not increase the number of stages of the OTA, which would also increase the power consumption. Since a limited output swing also affects the modulators performance, the combination of a large number of transistors stacked in the folded-cascode topology and the limited supply voltage of 1.8V, the PMOS cascode transistor was removed to allow more voltage headroom at the output of the amplifier based on what was done in (VAN DE VEL et al., 2009). The Common-Mode Feedback (CMFB) amplifier is necessary to guarantee the proper common-mode output level due to sensitive device properties and mismatch (RAZAVI, 2017). The common-mode reference is externally generated with a DC supply source.

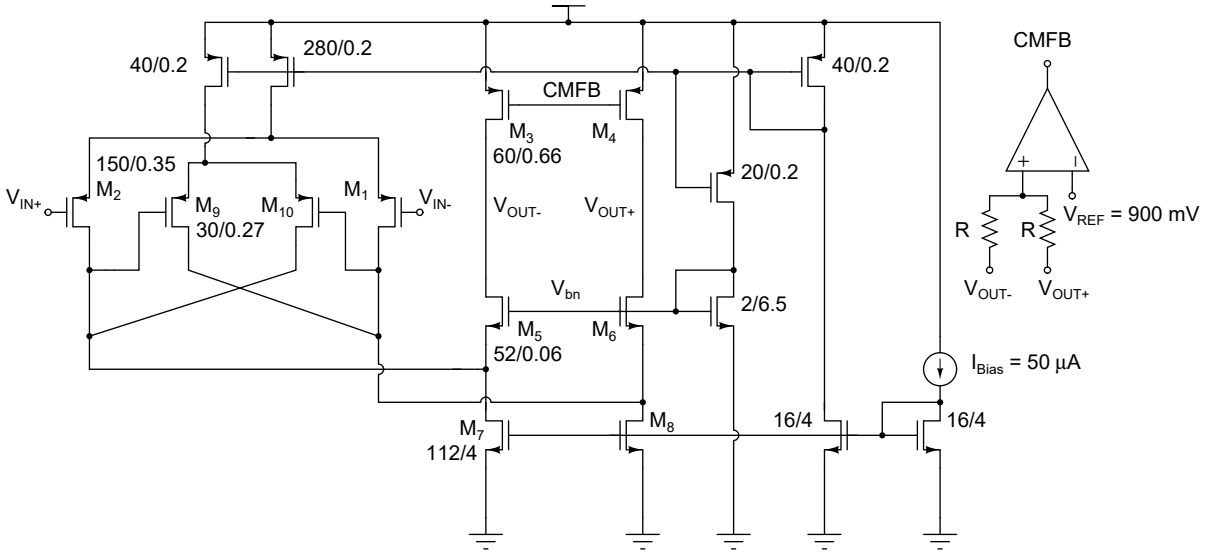


Figure 3.7: Fully differential folded-cascode amplifier with positive feedback gain enhancement and the CMFB.

From (MEZYAD M. AMOURAH, 2001) and the small signal analysis, the amplifier gain will be given by (3.11) where the cross-coupled pair M9 and M10 introduces a negative transconductance in the denominator.

$$A_1 \approx \frac{-g_{m1}g_{m7}}{g_{m5}(g_{m7} - g_{m9})} \tag{3.11}$$

From (3.11), when g_{m7} approaches g_{m9}, A_1 approaches ∞, implying that higher gains can be achieved due to the negative transconductance. Of course, this means that the input pair is extremely sensitive to mismatch and process variations. Considering that g_{m9} comes from a PMOS device and g_{m7} comes from a NMOS device, the matching cannot be made physically via placement of the devices, therefore, some form of calibration will have to be implemented.

The advantage of a single-stage OTA is that as a single-pole system it does not require a compensation capacitor to remain stable, and consequently there is no coupling of the compensation capacitor at the output stage, allowing for faster operation. In this case, the Slew-Rate will be given by

$$SR = I_{OUT}/C_L, \tag{3.12}$$

where I_{OUT} is the output current, and C_L is the load capacitance. The GBW is also very dependent on the output capacitance and is given by (ALLEN; HOLBERG, 2012)

$$GBW \approx \frac{g_{m1}}{2\pi C_L}. \tag{3.13}$$

From the equations above and the specifications defined in table 3.2 an initial estimation of transcoductances and device sizes can be obtained. Further refinements and final device sizings are defined through simulations.

3.3.2 Comparators

The comparator is one of the main blocks of a single-bit ΣΔM, however, due to its position in the modulator loop, the comparator specifications are not over demanding, as circuit errors are attenuated by the noise-transfer-function. According to (ROSA, 2018), typical static specifications require an offset and a hysteresis of the order of tens of mV, and a maximum comparison time of a quarter of the clock period. Considering, the maximum clock used (80 MHz), the comparison time should not exceed 3.125 ns.

Macro-Model

For the comparator, the behavioral model is taken from (ROSA, 2018) and is presented in the code listing 3.2. The comparison takes place during the strobe phase, after the positive clock edge. To avoid sudden changes in the output state, thus avoiding simulation errors, a hyperbolic tangent function, scaled by parameter *comp_slope* is used. The built in function, *transition*, controls other non-idealities such as rise time, fall time and comparison delay time.

Listing 3.2: Comparator pseudo code of in Verilog-A.

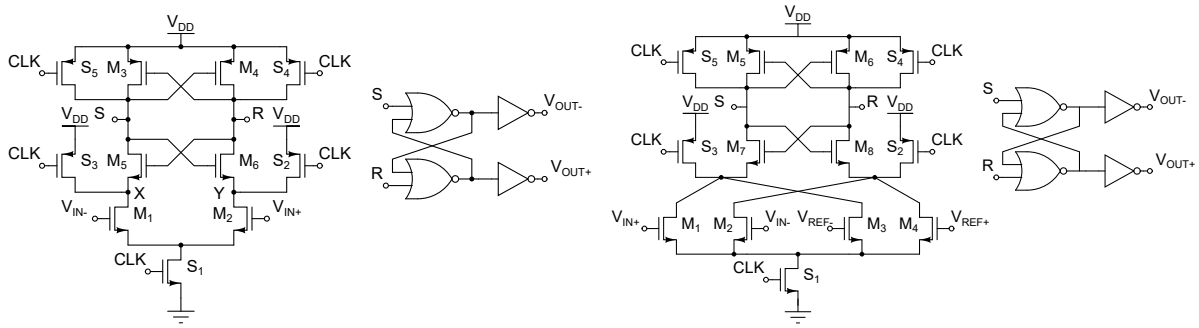
```
analog begin
  //Common mode definition
    vcm = (sigout_high + sigout_low)/2;
  //Comparison
  @(cross(V(STROBE) - threshold, +1, slack )) begin
    vout = (sigout_high - sigout_low) * tanh(comp_slope*(V(IN1_P,IN1_N)-V(IN2_P,IN2_N)
    -offset));
  end
  //Defining signal transition
  V(OUT_P, GNDA)<+vcm+transition(vout/2, td, tr, tf);
  V(OUT_N, GNDA)<+vcm-transition(vout/2, td, tr, tf);
end
```

Transistor Implementation

Fig. 3.8 shows the design of the comparator used, this topology is known as the StrongArm Latch (RAZAVI, 2015b). Fig. 3.8a depicts the comparator used as a single bit quantizer for

GSM operation and the first stage quantizer for UMTS operation, while Fig. 3.8b presents a modification with an additional input pair to be used in the multi-bit quantizer.

From Fig. 3.8a, its operation is as follows: initially CLK is at ground, therefore, S_1 is open, and S_{2-5} are all closed. During this time the nodes S, R, X and Y are all pre-charged with the supply voltage. When CLK changes to logic one, S_1 is turned on, and transistors $M1$ and M_2 will process the differential input, and generate a current proportional to the imbalance. This current allows the voltage difference in nodes X and Y ($|V_X - V_Y|$) to grow and possibly exceed $|V_{IN+} - V_{IN-}|$. Considering that M_{3-4} are initially off, the differential current will flow through the capacitance present at nodes X and Y, and will create a differential voltage between both nodes turning M_5 and M_6 on, starting the cross-coupled scheme, leading to a positive-feedback effect and, thus one of the outputs to V_{DD}. The output SR-latch maintains the output levels during the next reset phase.



(a) Comparator. (b) Extra input comparator.

Figure 3.8: Strong-Arm Latch (RAZAVI, 2015b) comparator. (a) With one differential input for the single-bit quantizer. (b) With extra differential pair for the multi-bit quantizer.

Table 3.3 presents the transistors sizings for the comparator of Fig. 3.8(a).

Table 3.3: Comparator transistor sizings (in μm).

Device	M1	M3	M5	S1	S3	S5
Size (W/L)	0.8/1	0.8/1	0.8/1	1/0.26	1/0.26	1/0.26

3.3.3 Multi-bit Quantizer

The multi-bit quantizer is used to convert the output of the modulator either in BT or UMTS modes to the digital domain and reconverts to the analog domain to be fed back to the modulator, essentially performing an analog-to-digital-to-analog (A/D/A) operation.

The 5-level quantizer is built in circuit form using Verilog-A models of the comparator and switches. The complete circuit is presented in Fig. 3.9. A resistor ladder defines the 4 threshold levels to be compared with the inputs, resulting in a 5 output digital word defined by D_0 to D_4. The resistor ladder is shared with the D/A converter which also defines the 5 levels of the output analog domain defined by the DAC+ and DAC- pins.

The ladder uses poly-resistors of 400 Ω and the references V_{REF+} and V_{REF-} are 1.4 V and 400 mV respectively, defining the modulator full-scale range.

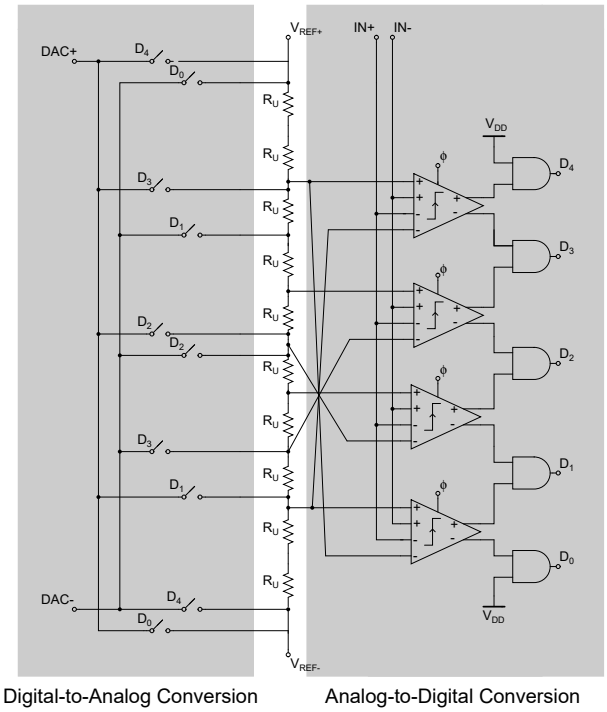


Figure 3.9: Circuit implementation of the 5-Level quantizer.

3.3.4 Switches

In switched-capacitor based circuits, the switches on-resistance (R_{on}) non-linearity and elevated values may impact severely the circuit linearity (WEI YU; SUBHAJIT SEN; LEUNG, 1999). In ΣΔ Modulators, the impact comes in the harmonic distortion caused mainly by the third harmonic component. From (ROSA, 2018) and (RAZAVI, 2015c), the third-harmonic distortion of a sampling capacitor C_S with on-resistance R_{on} is given by

$$H_{D3} \approx \frac{\pi f_{in} C_s R_{on}}{2(V_{ON} - Vth)^2} A_{in}^2. \tag{3.14}$$

Where f_{in} is the input frequency, V_{ON} is the switch on voltage, V_{th} is the threshold voltage and A_{in} is the input signal amplitude.

Macro-Model

The non-ideal switch equivalent circuit is presented in Fig. 3.10. When the clock signal is low it works as a very high resistance, when it is high it behaves as a low resistance. The Verilog-A is very simple and presented in listing 3.3.

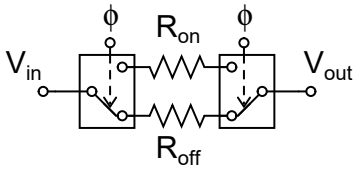


Figure 3.10: Macro-model of the switch.

Listing 3.3: Pseudo code of the switch in Verilog-A.

```
analog begin
  @(initial_step("ac", "dc", "tran", "xf" )) begin
    rout = roff;
  end
  @( cross ( V(CLK, GND) - threshold - halfhys , +1, slack, CLK.potential.abstol))
    rout = ron;
  @( cross ( V ( CLK, GND ) - threshold + halfhys, -1, slack, CLK.potential.abstol))
    rout = roff;
  i_aux = V(IN, OUT)/rout;
  I(IN, OUT) <+ i_aux;
end
```

Transistor Implementation

Fig. 3.12 shows the design of the switches used in the modulator. The transmission gate is shown in Fig. 3.12b and is a parallel combination of a NMOS and a PMOS switch. The on-resistance of a NMOS is defined by (3.15), while the on-resistance of PMOS switch is given by (3.16). It is clear that for the NMOS switch when V_{gs} approaches V_{th}, the on-resistance rises to infinity. For the PMOS switch the same thing happens when V_s (or V_{IN}) approaches V_{th} (V_g is 0 V when the PMOS switch is on). Therefore, the parallel combination of these two switches never result in a on-resistance that is extremely high, however it is still very non-linear, as depicted in Fig.3.11 (RAZAVI, 2017).

$$R_{on,N} = \frac{1}{\mu_n C_{ox}(W/L)_N(V_{DD} - V_{IN} - V_{th,N})} \tag{3.15}$$

$$R_{on,P} = \frac{1}{\mu_p C_{ox}(W/L)_P(V_{IN} - |V_{th,P}|)} \tag{3.16}$$

Fig. 3.11 also shows the non-linear resistance region in which the input signal will operate to illustrate the cause of distortion in the output spectrum.

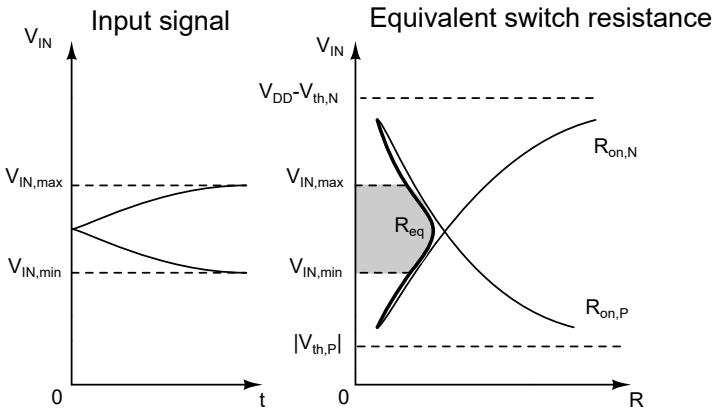


Figure 3.11: Input signal amplitude and equivalent resistance of the transmission gate.

To avoid the non-linearity of the input signal, bootstrapping was implemented for the input switches of the modulator. The bootstrapped (Fig. 3.12a) design was taken from (RAZAVI, 2015a), and uses a capacitor C_b to store the logic one voltage, and maintain a constant V_{gs} in M_1, therefore, improving its linearity.

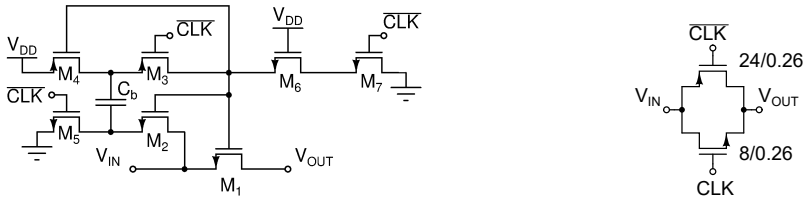


Figure 3.12: Switches used in the modulator. (a) Input switches (Bootstrapped switch). (b) Every other switch (Transmission gate).

Table 3.4 presents the sizings of the bootstrapped switch. The transmission gate sizings are presented in Fig. 3.12(b).

Table 3.4: Bootstrapped switch transistor sizings (in μm).

Device	M1	M2	M3	M4	M5	M6	M7
Size (W/L)	1/0.26	1/0.26	1/0.26	1/0.26	1/0.26	1/0.26	1/0.26

Table 3.5: PLL frequency requirements.

Standard	**ADC Type**	**Sampling Freq.**	**Bandwidth**	**Max. Jitter**
GSM	ΣΔ	40 MHz	200 kHz	≤10 ns
Bluetooth	ΣΔ	60 MHz	500 kHz	≤5 ns
UMTS	ΣΔ	2 MHz	80 MHz	≤3 ns
DVB-S2 Mode 1	Pipeline	80 to 120 MHz	80 to 120 MHz	≤50 ps
DVB-S2 Mode 2	Pipeline	160 to 200 MHz	160 to 200 MHz	≤30 ps

3.4 PLL-Based Clock Synthesizer

The clock synthesizer was originally developed for a Pipeline ADC with nominal frequency of 200 MHz for a project at the Eldorado Research Institute (specifically for a digital TV receiver with Digital Video Broadcasting - Satellite - Second Generation (DVB-S2) standard) and is repurposed for this project. The topology chosen is Phase-Locked Loop-based and for this project frequency dividers were necessary to achieve the required frequencies for the ΣΔM as shown in table 3.5.

The main bottleneck of clock synthesizers in high-speed state-of-the-art ADCs is the jitter (RAZAVI, 2021). Jitter requirements of table 3.5 are taken from (3.17), based on (REDMAYNE; TRELEWICZ; SMITH, 2006)

$$SNR = -20log(2\pi f_{in}\sigma) \tag{3.17}$$

where SNR is the ADCs Signal-to-Noise Ratio, f_{in} is the maximum input frequency and σ is the rms jitter.

Since the output data rate of the proposed ΣΔM is not high, the jitter requirements are relaxed and not hard to achieve. Therefore, a simple PLL topology with N-integer frequency divider and a second-order loop filter was chosen.

The complete diagram of the proposed PLL is shown in Fig. 3.13 and its operation is as follows: first F_{REF} of 10 MHz is compared with the feedback F_{DIV} frequency, which is the output VCO frequency F_{VCO} divided by the Pulse-Swallow Frequency Divider (PSFD). The comparison result is fed to the Charge Pump (CP) circuit, which injects or removes charge in

the Loop Filter (LF), altering the control voltage V_{CONT}. This feedback scheme controls the VCO output frequency, until the system reaches equilibrium. The output VCO frequency can also be divided by two, three or four, resulting in F_{OUT}.

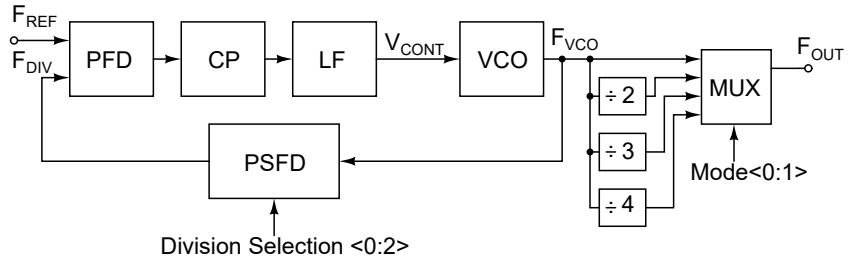


Figure 3.13: PLL architecture block diagram.

3.4.1 PLL Feedforward Path (PFD, CP, LF and VCO)

The designs of the Phase and Frequency Detector (PFD), CP, LF and VCO are shown in Fig. 3.14. The first sub-circuit of the PLL system is the PFD. As the name implies, it detects the phase and frequency from two waveforms A and B shown in Fig. 3.14. It is a simple and robust design consisting of two resettable D flip-flops controlled by an AND gate, taken from (RAZAVI, 2020).

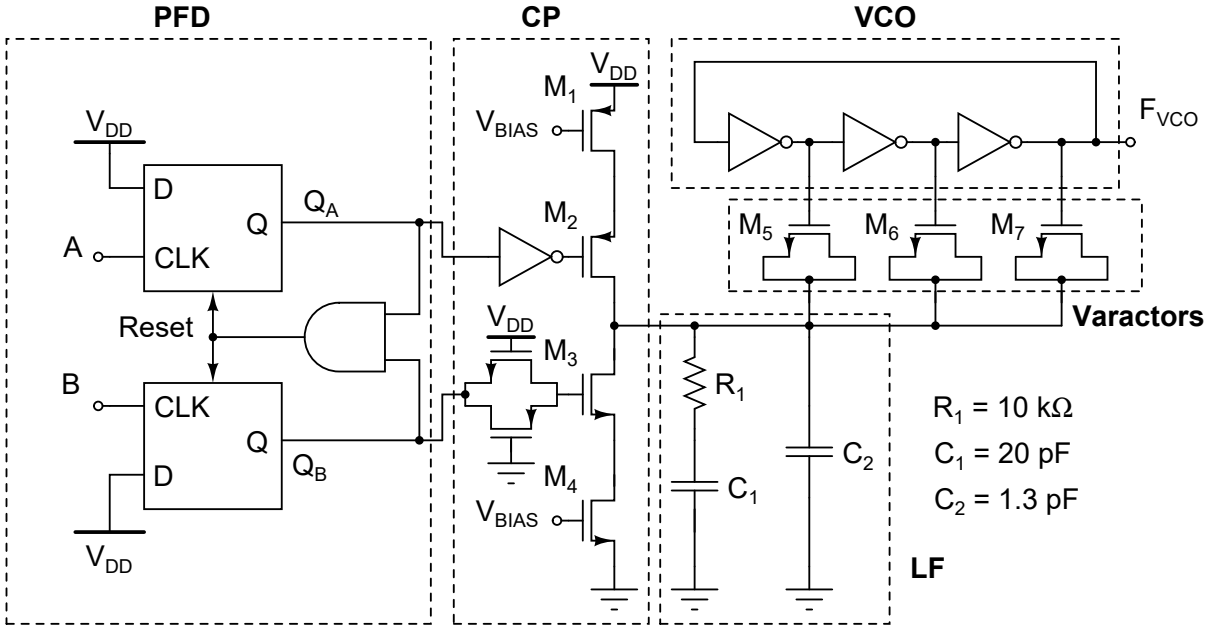


Figure 3.14: PLL feedforward path: PFD, CP, LPF and VCO.

After the phase and frequency detection performed by the PFD, the signals Q_A and Q_B control if the CP sinks our sources charge in the LF. An always on transmission gate was

used at the input Q_B to avoid skewing due to the delay introduced by the inverter at the Q_A input and therefore equalizing the delays in both control switches. To avoid the imbalance of the up and down currents wider transistors were chosen for the current sources. The increased capacitance from larger transistor did not impact the PLL operation as the synthesized frequencies are not very high (RAZAVI, 2020).

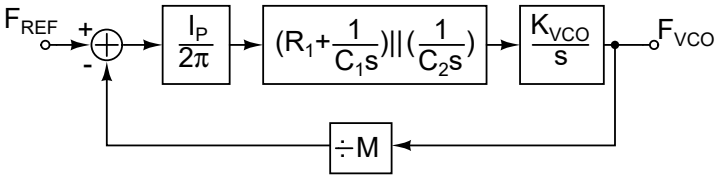


Figure 3.15: PLL linear model: frequency domain representation.

The basic idea of the capacitor C_1 is to store or release the charge coming from the CP, and control the voltage V_{CONT}. The VCO adds another pole at the origin, thus, through the addition of resistor R_1 in series with C_1, the loop is stabilized with the addition of a zero at $-1/R_1C_1$. The addition of R_1 introduces a ripple in the V_{CONT} waveform, and hence spurs in the spectrum. The magnitude of the ripple is proportional to the resistor size and the current coming from the CP. To reduce the ripple, the capacitor C_2 is introduced. Choosing $C_2 \leq 0.2C_1$, the closed loop transfer function settling behavior is negligibly affected (RAZAVI, 2020), this way, a second order system where C_2 is not considered, becomes a good approximation for hand written calculations during the design phase to predict settling time, stability, maximum overshoot and other parameters. Based on the linear model of Fig. 3.15, its open loop transfer function can be written as (3.18)

$$H(s) = \frac{K_{VCO}I_p}{2\pi Ms}K(s), \tag{3.18}$$

where K_{VCO} is the VCO gain, I_p is the CP current, M is the division ratio of the PLL and K(s) is the loop filter impedance, given by the parallel combination of $(R_1 + 1/(C_1s))$ and $1/(C_2s)$

$$K(s) = \frac{R_1C_1s + 1}{R_1\frac{C_1C_2}{C_1+C_2}s + 1}\frac{1}{(C_1 + C_2)s}. \tag{3.19}$$

With the addition of C_2, a third pole is added to the transfer function frequency response at

$$|\omega_{p3}| = \left(R_1\frac{C_1C_2}{C_1 + C_2}\right)^{-1}, \tag{3.20}$$

resulting in the following phase margin

$$PM = tan^{-1}(R_1 C_1 \omega_u) - tan^{-1}\left(R_1 \frac{C_1 C_2}{C_1 + C_2}\omega_u\right), \tag{3.21}$$

where ω_u is the unit gain bandwidth frequency.

One of the requirements during development of the DVB-S2 SoC project was a small area availability for the PLL clock synthesizer. Thus an optimum choice of VCO topology is the inverter-based voltage-controlled ring oscillator (VCRO) as it will combine small area and low power consumption with sufficient phase noise response. Three inverters are connected in series, with the output of the third inverter connected to the input of the first. The oscillation frequency control is made by the source-gate-bulk voltage in the n-type MOSFET varactors connected to each inverter output. The varactors decrease in capacitance as V_{CONT} (Fig. 3.14) increases, hence the oscillator frequency increases. Table 3.6 presents the relevant devices sizings used in the feedforward path from Fig. 3.14.

Table 3.6: PLL feedforward path relevant transistor sizings (in µm).

Device	M1	M2	M3	M4	M5	M6	M7
Size (W/L)	128/2	3/0.3	2/0.06	20/1	6/3	6/3	6/3

3.4.2 Programmable Loop Frequency Divider

From the specifications defined by table 3.5, an integer-N second order PLL-based frequency synthesizer is a proper structure to obtain all desired frequencies.

Macro-Model

The frequency code snippet is shown in listing 3.4. The divide ratio is defined by the bits D[0] to D[2] and range from 16 to 23 (next section explains in detail why this divide range). Then, the built-in *cross* function counts the transitions of the input clock. Based on the previously defined divide ratio, the input frequency is divided, including delay time (*td*) and transition time (*tt*) for the output clock.

Transistor Implementation

Listing 3.4: Snnipet of the Programmable Frequency Divider code in Verilog-A.

```
analog begin
  if(V(D[0])<vth && V(D[1])<vth && V(D[2])<vth)
    ratio = 16;
  else if(V(D[0])>vth && V(D[1])<vth && V(D[2])<vth)
    ratio = 17;
  else if(V(D[0])<vth && V(D[1])>vth && V(D[2])<vth)
    ratio = 18;
  else if(V(D[0])>vth && V(D[1])>vth && V(D[2])<vth)
    ratio = 19;
  else if(V(D[0])<vth && V(D[1])<vth && V(D[2])>vth)
    ratio = 20;
  else if(V(D[0])>vth && V(D[1])<vth && V(D[2])>vth)
    ratio = 21;
  else if(V(D[0])<vth && V(D[1])>vth && V(D[2])>vth)
    ratio = 22;
  else if(V(D[0])>vth && V(D[1])>vth && V(D[2])>vth)
    ratio = 23;
  else
    ratio = 16;
    @(cross(V(FIN) - vth, dir)) begin
  count = count + 1; // count INput transitions
  if (count >= ratio)
      count = 0;
  n = (2*count >= ratio);
    end
    V(FOUT) <+ transition(n ? vh : vl, td, tt);
end
```

A common implementation of an integer-N divider is the Pulse Swallow Frequency Divider topology, which allows for a modular design of the programmable divider. The overall divide ratio ($M = F_{IN}/F_{OUT}$) can be adjusted by a 3 bit input of a programmable counter named Swallow Counter (SC) in Fig. 3.16.

The operation of the PSFD works as follows: initially P and S are reset and the frequency at A is equal to $F_{VCO}/(N+1)$. After $(N+1)S$ pulses, the SC changes B to HIGH. Now the frequency at A is equal to F_{VCO}/N. After $(P-S)$ pulses at A, or $(P-S)N$ input cycles, P goes HIGH and resets the SC, restarting the process. Therefore, one pulse is generated at the ouput for every $(N+1)S + (P-S)N$ input pulses. The resulting output frequency is $F_{DIV} = F_{VCO}/(NP+S)$ as long as $P > S$ (RAZAVI, 2020).

In this design the values N, P and S are 2, 8 and 7 respectively, allocating three bits for the SC control and allowing the reference frequency to be multiplied by 16 up to 23.

The Dual Modulus Prescaler (DMP) is shown in Fig. 3.17 and consists of a modified divide by 3 with a modified logic to accommodate an external selection bit. When Modulus Control (MC) is HIGH, FF_1 has no effect and the circuit divides by 2. If MC is LOW, the circuit divides

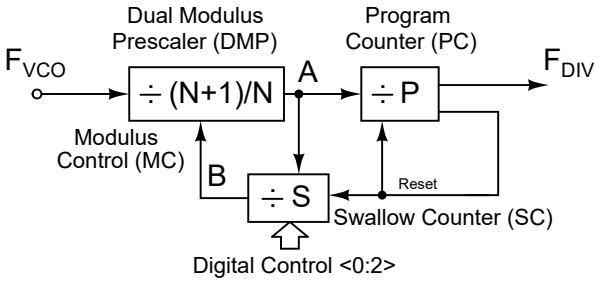


Figure 3.16: Pulse Swallow Frequency Divider (PSFD) architecture.

by 3. Fig. 3.17 also presents the SC design, it is a slight variation from the design present in (RAZAVI, 2020). The input frequency is counted from 000 up to the word defined by D<0>, D<1> and D<2>. Then, it changes the output to HIGH, altering the DMP division, disabling all dividers while it retains the output on HIGH until the Program Counter (PC) resets all dividers. Now the output returns to LOW and the process is repeated. The PC is a simple divide by 8 circuit with an end of count reset, also shown in Fig. 3.17.

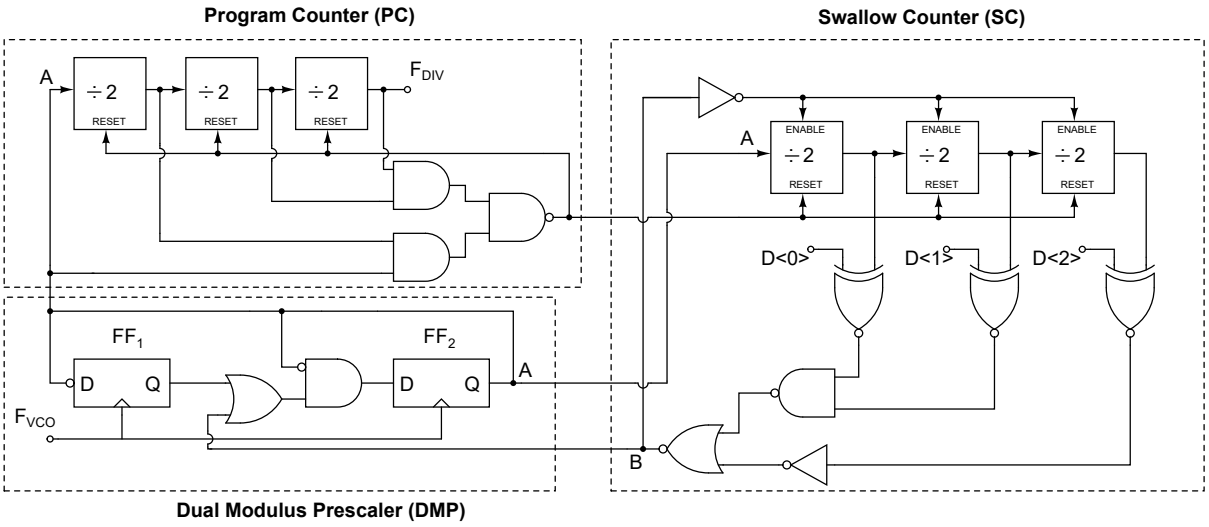


Figure 3.17: Complete design of the pulse swallow divider.

3.5 Auxiliary Blocks

3.5.1 D Flip-Flops

D-Type Flip-Flops are used throughout the design the PLL-based clock synthesizer digital circuitry, specifically the dividers, the PSFD and the PFD.

All flip-flops used are shown in Fig.3.18. The positive-edge D flip-flop from Fig.3.18a is taken from (BROWN; VRANESIC, 2013). A modification to allow for Preset and Clear

operations, also taken from (BROWN; VRANESIC, 2013), is presented in Fig.3.18b. Fig.3.18c shows the inclusion of an Enable logic to allow the operation of the Swallow Counter of Fig.3.17. Fig.3.18d (taken from (RAZAVI, 2020)) shows the ressetable latch used only in the PFD of Fig.3.14. Tables 3.7a to d present the truth tables of the flip-flops of Fig.3.18.

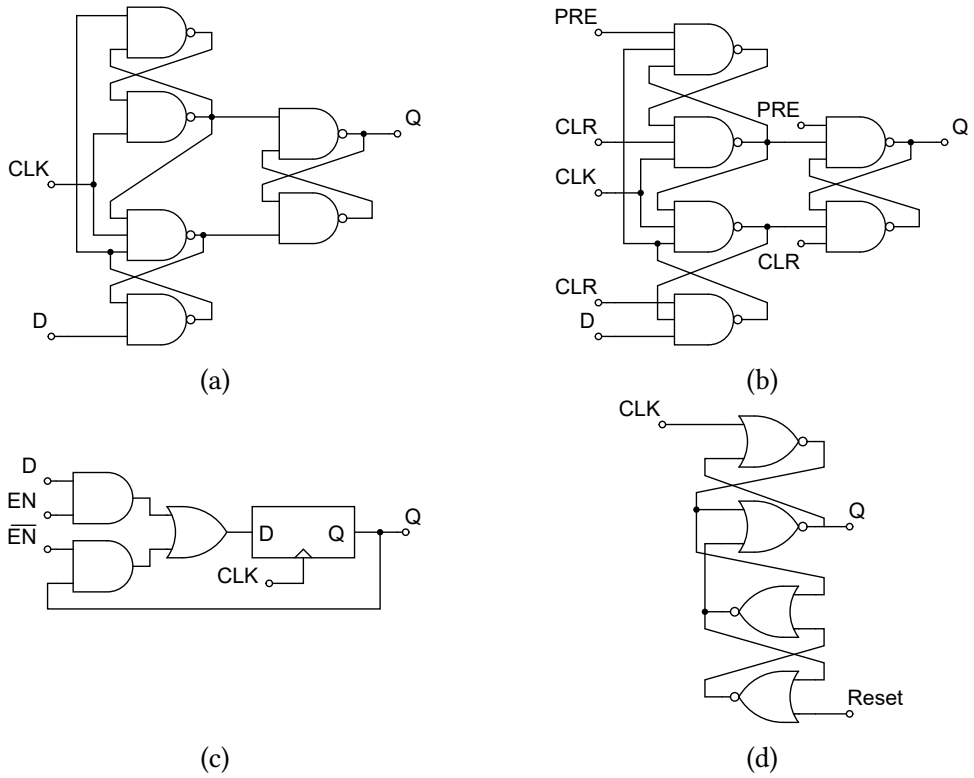


Figure 3.18: Flip-Flops used for the frequency dividers and other digital circuitry. (a) D Flip-Flop; (b) D Flip-Flop with Preset and Clear pins; (c) D Flip-Flop with Enable pin; (d) ressetable D-type latch (for the PFD of Fig.3.14).

3.5.2 Frequency Dividers

The divide-by-two and divide-by-three circuits are presented in Figs.3.19 and 3.20 respectively. Both designs are taken from (RAZAVI, 2020).

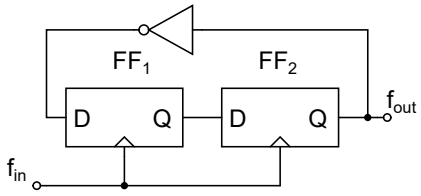


Figure 3.19: Divide-by-two circuit.

Table 3.7: D-Type flip-flops truth tables. (a) Fig.3.18a; (b) Fig.3.18b; (c) Fig.3.18c; and (d) Fig.3.18d.

(a)

Inputs		Outputs	
CLK	D	Q	$\overline{Q}$
↑	1	1	0
↑	0	0	1
0	X	Q_0	$\overline{Q_0}$

(b)

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	$\overline{Q_0}$

(c)

Inputs			Outputs	
EN	CLK	D	Q	$\overline{Q}$
0	X	X	Q_0	$\overline{Q_0}$
1	↑	1	1	0
1	↑	0	0	1
1	0	X	Q_0	$\overline{Q_0}$

(d)

Inputs		Outputs
$\overline{RESET}$	CLK	Q
0	X	0
1	↑	1
1	0	Q_0

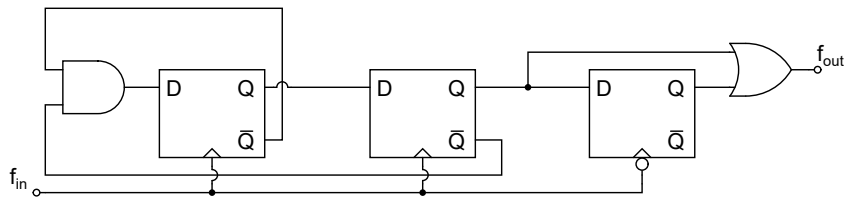


Figure 3.20: Divide-by-three circuit.

3.5.3 Non-Overlapping Clock Generation and Buffering

Generally in switched-capacitor circuits two phases of non-overlapping clocks are required to avoid unwanted charge transfer during sampling and transfer stages. A common design of implementation of non-overlapping clock phases ϕ_1 and ϕ_2 is shown in Fig. 3.21. Additional phases ϕ_3 and ϕ_4 are delayed versions of ϕ_1 and ϕ_2.

To drive large capacitors in the ADCs the clock phases require proper buffering. This is achieved by the buffer tree shown in Fig. 3.22 for each phase (ROSA, 2018).

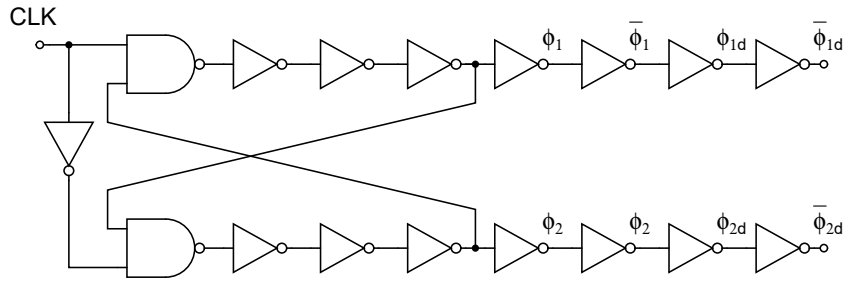


Figure 3.21: Non-Overlapping clock generation.

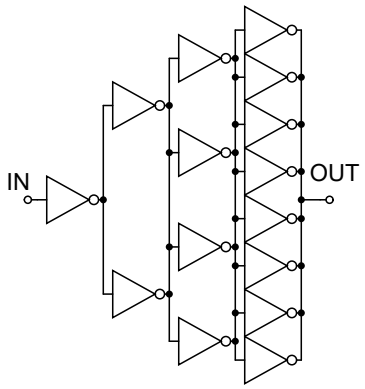


Figure 3.22: Buffer tree for each clock phase.

3.5.4 Bias Current Generation

To generate both the charge pump currents, and the bias currents for the operational amplifier, a current source is necessary. The design is shown fig. 3.23. It is the well-know supply-independent self-biased current source presented in (RAZAVI, 2017) where a feedback between a PMOS and NMOS current mirrors bias each other generating a well defined current reference independent from supply voltage variation. The output current can be inferred by the voltage drops in the loop defined by M_1, M_2 and R as stated by (3.22):

$$\frac{V_{GS1} - V_{GS2}}{R} = I_{OUT}. \tag{3.22}$$

Therefore, the output current is (3.23)

$$I_{OUT} = \frac{2}{\mu_n C_{ox}(W/L)_N R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2. \tag{3.23}$$

Ideally as described by (3.22) and (3.23), the output current is independent from the supply voltage. In practice, this is not true due to channel modulation (RAZAVI, 2017).

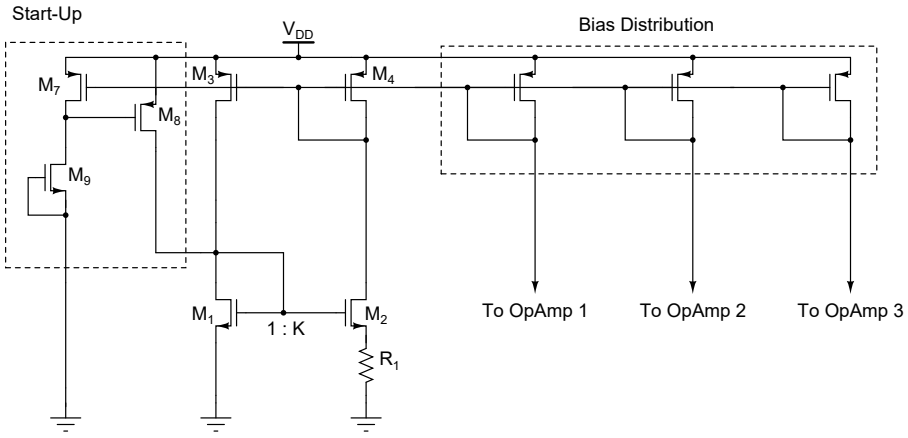


Figure 3.23: Current source design.

The main disadvantage of this topology is the existence of a "degenerate" bias point (RAZAVI, 2017), meaning that there are two states possible for operation: 1) the previously described state where it is assumed that current is flowing through the transistors, and 2) a state where no current is generated and the circuit does not turn on. To avoid the second state, a start-up circuit is necessary. The start-up operation is as follows: as the supply voltage starts increasing, transistor M_8 turns-on and a small current will flow from source to drain forcing an initial current in the feedback circuit composed by M_1, M_2, M_3 and M_4, rendering the "degenerate" bias point impossible. With the current flowing in the circuit, M_7 will copy the current from M_3 and charge the capacitance of M_9, increasing the voltage drop across M_9 turning M_8 off, and leaving M_7 in the triode region with a negligible quiescent current.

3.6 Summary

This section presented the design techniques used in the ΣΔM, including the circuit and Verilog-A implementation of the main sub-circuits, such as 1) OTA, 2) Comparators, 3) Multi-bit quantizer, 4) Switches and 5) the complete clock synthesizer. Details in the challenges faced during the design phase was described with the inclusion of the insight gained during the integration of each sub-circuit in the system top.

The next section will detail the results obtained for each system (ΣΔM and PLL Clock Synthesizer), highlighting key results of main sub-circuits.

Chapter 4

Results

This section presents the results obtained for the ΣΔM and Clock Synthesizer, also highlighting the results for the main sub-circuits present in both systems. All results obtained from simulations were performed using the Cadence Virtuoso Analog Design Environment and its related software ecosystem. Results from the ΣΔM and its sub-circuits are from transistor-level schematic simulations. Results from the PLL clock synthesizer and its sub-circuits are from extracted layout simulations with the exception of the phase noise curve and frequency range sweep which were obtained from chip measurements.

4.1 Layout

4.1.1 ΣΔ Modulator

The complete layout floorplan for the project is presented in Fig. 4.1. It is heavily based on the recommendations of (ROSA, 2018) where the modulator is separated in three different regions: 1) the digital region (containing the clock synthesizer, the non-overlapping clock generator, the clock buffers and the clock bus); 2) the mixed-signals region (containing the integrator switches); and 3) the analog region (containing the operational amplifiers, the integrators capacitors, the current bias generator and the analog buses). These three regions are separated by both an N-type guard ring and a P-type guard ring to reduce noise propagation coming from the high-frequency switching of the clock generation and its buses coupling through the substrate. This noise can affect the analog region and consequently reduce the SNR. As expected from the complete schematic view of the modulator in Fig. 3.5 of Section 3, there are clock signals, analog signals, bias currents, voltage references and

supply buses throughout the whole circuit, rendering high complexity to the layout. To avoid a labyrinth of unorganized connections one goal is to clearly define the major buses of the system. In this project a total of 8 clock phases with high driving capacity were necessary (ϕ_1, $\overline{\phi_1}$, ϕ_2, $\overline{\phi_2}$, ϕ_{1d}, $\overline{\phi_{1d}}$, ϕ_{2d}, $\overline{\phi_{2d}}$), requiring thick metal paths. To encompass the whole circuit, a "C" shaped bus was implemented. Similarly the analog buses also reach the majority of the analog region, therefore two buses were implemented, and the same was done for the supply and ground buses.

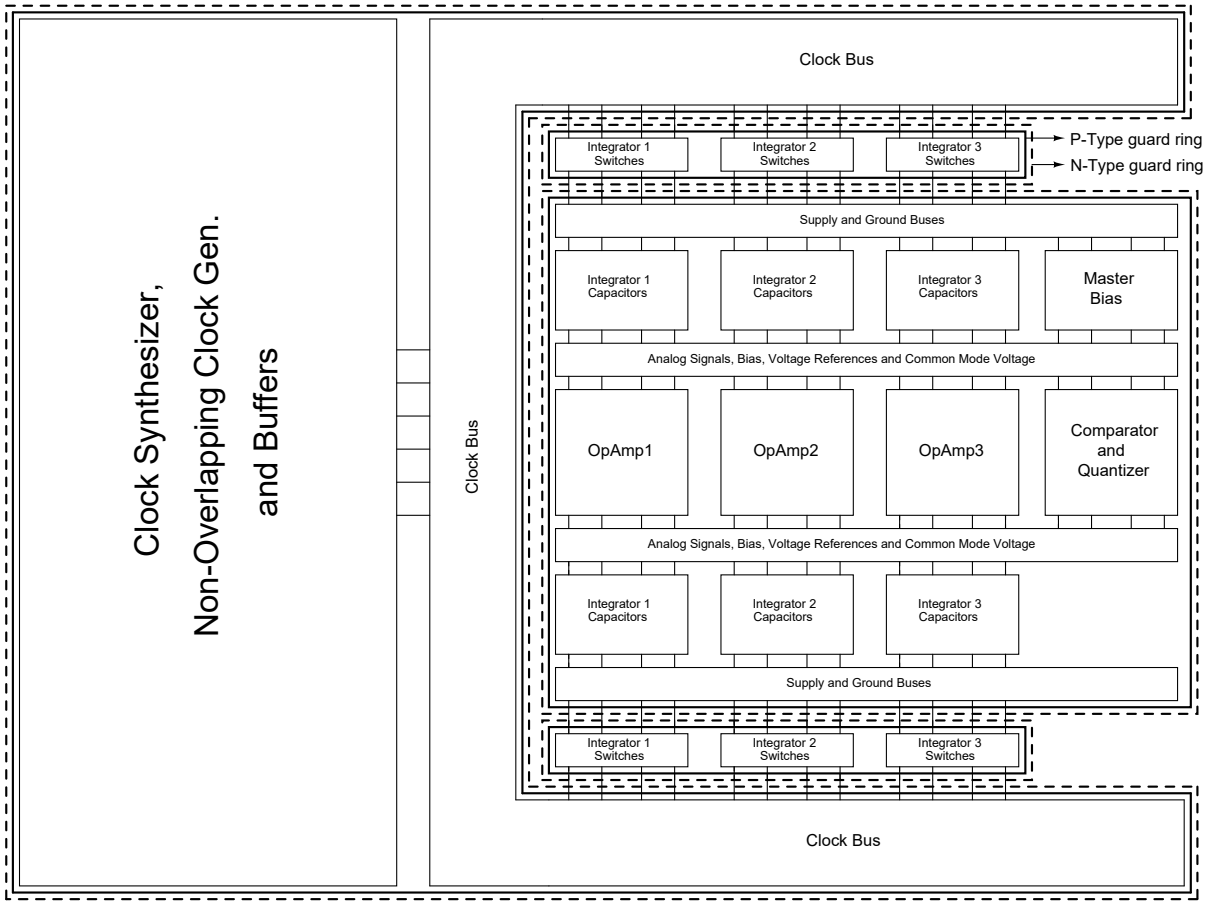


Figure 4.1: ΣΔM floorplan.

4.1.2 Clock Synthesizer

The layout floorplan for the Clock Synthesizer is depicted in Fig. 4.2. No particular noise suppression technique was used in this floorplan since every sub-circuit of the PLL is subjected to high frequency signals. The only exception is the CP current generator which was protected by both an N-type and a P-type guard ring. The major constraint for this layout was the area availability, so the main objective in the floorplanning was related to area reduction. The complete layout of the PLL is shown in Fig. 4.3. Half the area is composed by the capacitor

C_1 with a value of approximately 20 pF. The capacitors are Metal-oxide-metal type, and range from the first layer of metal up to the seventh. This type of capacitor presents the highest capacitance per area. The technology allows for 9 layers of metal, however metals 8 and 9 were reserved for the top system layout. The die micrograph and the zoomed-in-view of the PLL are shown in Fig. 4.4. Due to the required metal density conditions of the process, the metal layers block the semiconductor layers (known as the Front-End of Line - FEOL), when viewed from a microscope. From the figure, only the capacitors are identifiable.

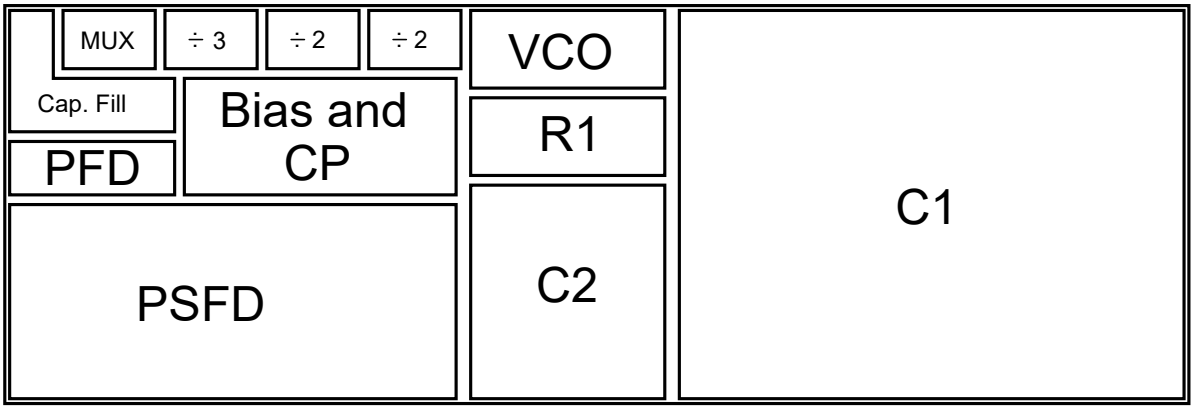


Figure 4.2: PLL floorplan.

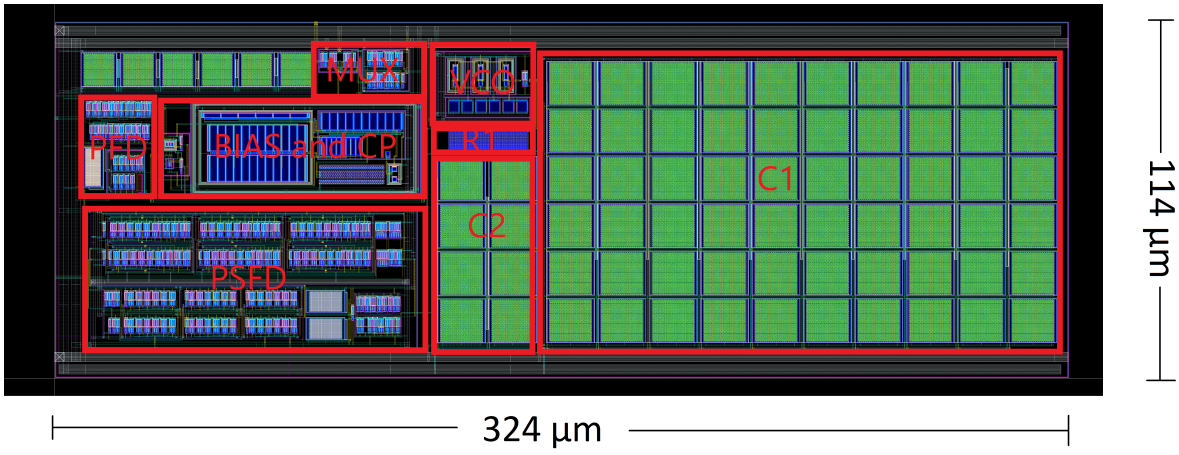


Figure 4.3: Clock synthesizer layout.

For testability purposes, only a digital multiplexer was placed at the output of the PLL to provide an external clock to the ADC in case the PLL fails. This was an oversight during the design and planning phase, and luckily, did not result in major issues since the fabricated PLL worked. A simple technique to evaluate internal nodes of a circuit is to multiplex digital signals through digital multiplexers, and analog signals through analog multiplexers. This way, it is

possible to verify several internal nodes with only two external pads for a more consistent IC design and verification methodology and gain more insight on the possible failure mechanisms of an unsuccessful tape-out. Additionally, test-points in the layout are also recommended if a probe station is available during measurements.

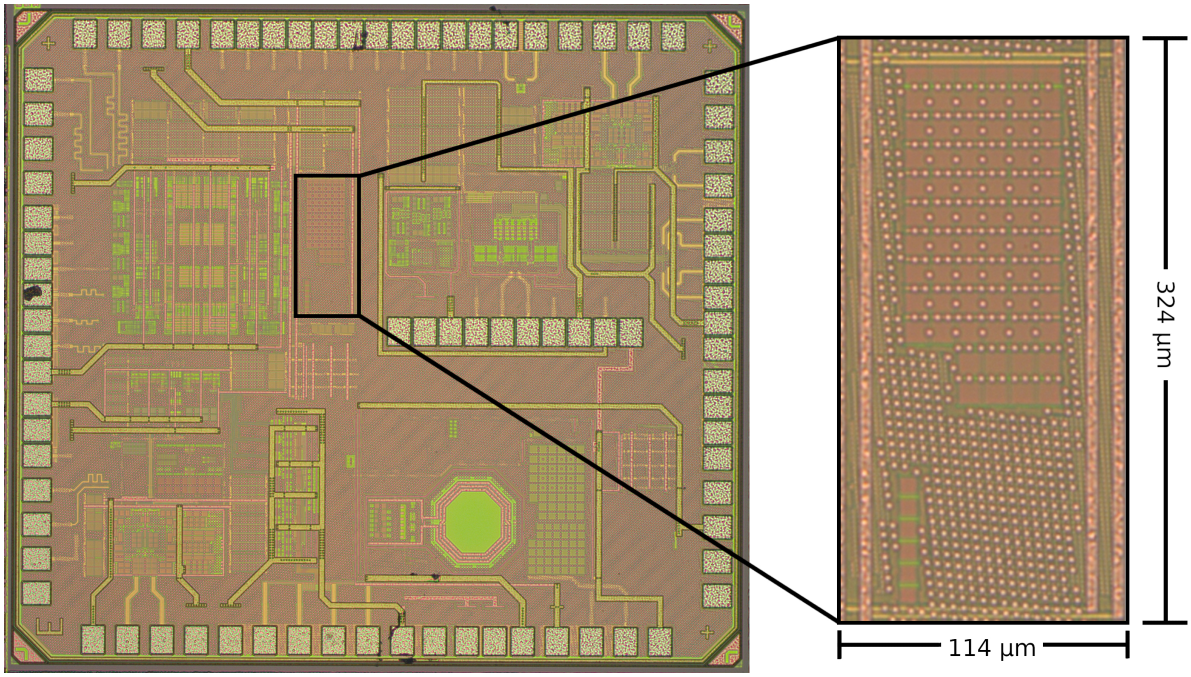


Figure 4.4: Die micrograph of the 65-nm chip with a zoomed-in view of the PLL occupying an area of 0.037 mm^2.

4.2 Reconfigurable ΣΔ Modulator

This section highlights the obtained results of the ΣΔM main sub-blocks, the PLL clock synthesizer system and its main sub-blocks, and at the end, the overall modulators performance. Comparisons with other works are shown for the Clock Synthesizer and the ΣΔM.

4.2.1 OTA

The OTA is one of the most critical sub-circuits of the ΣΔM, its characterization must be thorough with both AC, DC and transient performance. Fig. 4.5 depicts all test-benches used for amplifier.

The voltage defined for the ΣΔM is 1.8 V, however during the development a mistake was made where the sub-circuits were developed using transistors rated for 1.2 V. This was

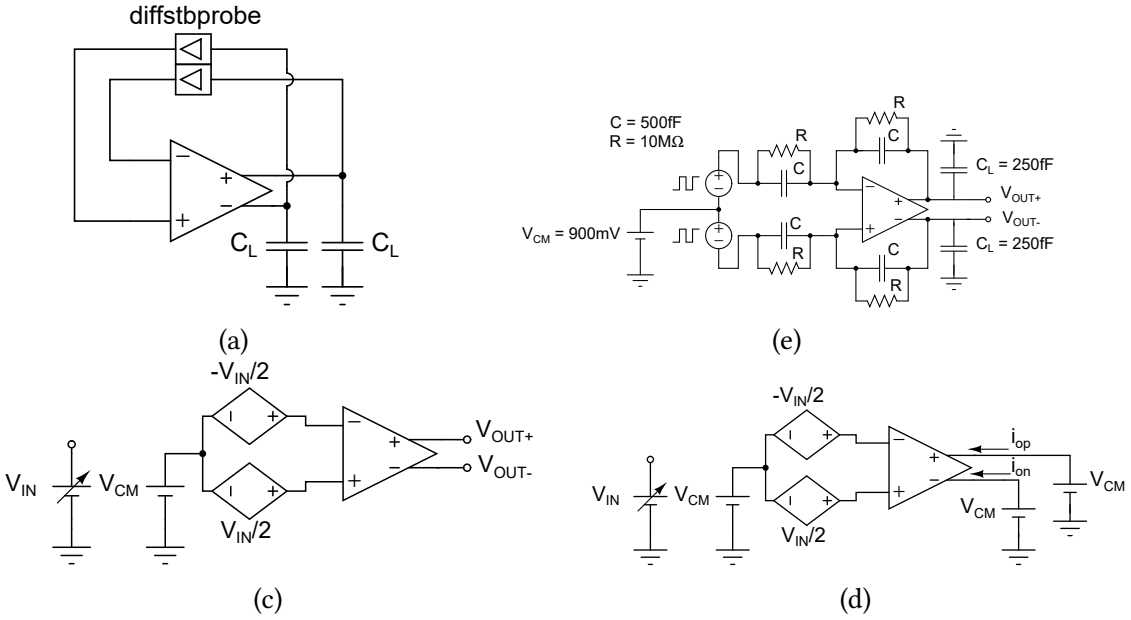


Figure 4.5: Operational amplifier test-benches. (a) Stability/freq. response; (b) slew rate; (c) differential output voltage; (d) differential output current and transconductance.

corrected for every sub-circuit of the ΣΔM and the results highlighted in this section are for the 1.8 V transistor. The only exception is the OTA. A lot of effort was spent trying to achieve the requirements defined in table 3.2, however they were not met. For this reason, exceptionally for the OTA, the results for the implementation with 1.2 V and 1.8 V transistors will be highlighted. The results employing both OTAs will also be highlighted with their integration in the ΣΔM at the end of this section.

It is important to note that the breakdown voltage of the 1.2 V transistors is at around 9 V. The technology used is rated for 1.2 V applications, offering a wide range of transistors (low V_{th}, normal V_{th}, high V_{th}, etc.) for this supply. For higher voltages such as 1.8 V, 2.5 V and 3.3 V the transistor options are very limited making the development more difficult for higher voltages.

To obtain the open-loop frequency response of the amplifier, the test-bench of Fig. 4.5a was used with a stability (stb) analysis to evaluate 1) the DC gain, 2) the GBW and 3) the phase margin. The frequency magnitude response is shown in Fig. 4.6a and Fig. 4.6b for the OTA with 1.2 V MOSFETs and the OTA with 1.8 V MOSFETs respectively, and the phase frequency response is shown in Fig. 4.6c and Fig. 4.6d for the OTA with 1.2 V MOSFETs and the OTA with 1.8 V MOSFETs respectively. To verify the circuits performance for process variation, a Monte Carlo analysis with 2200 samples was performed only in the OTA with 1.2 V transistors. The high number of samples ensures a 95% confidence level for 3σ variation

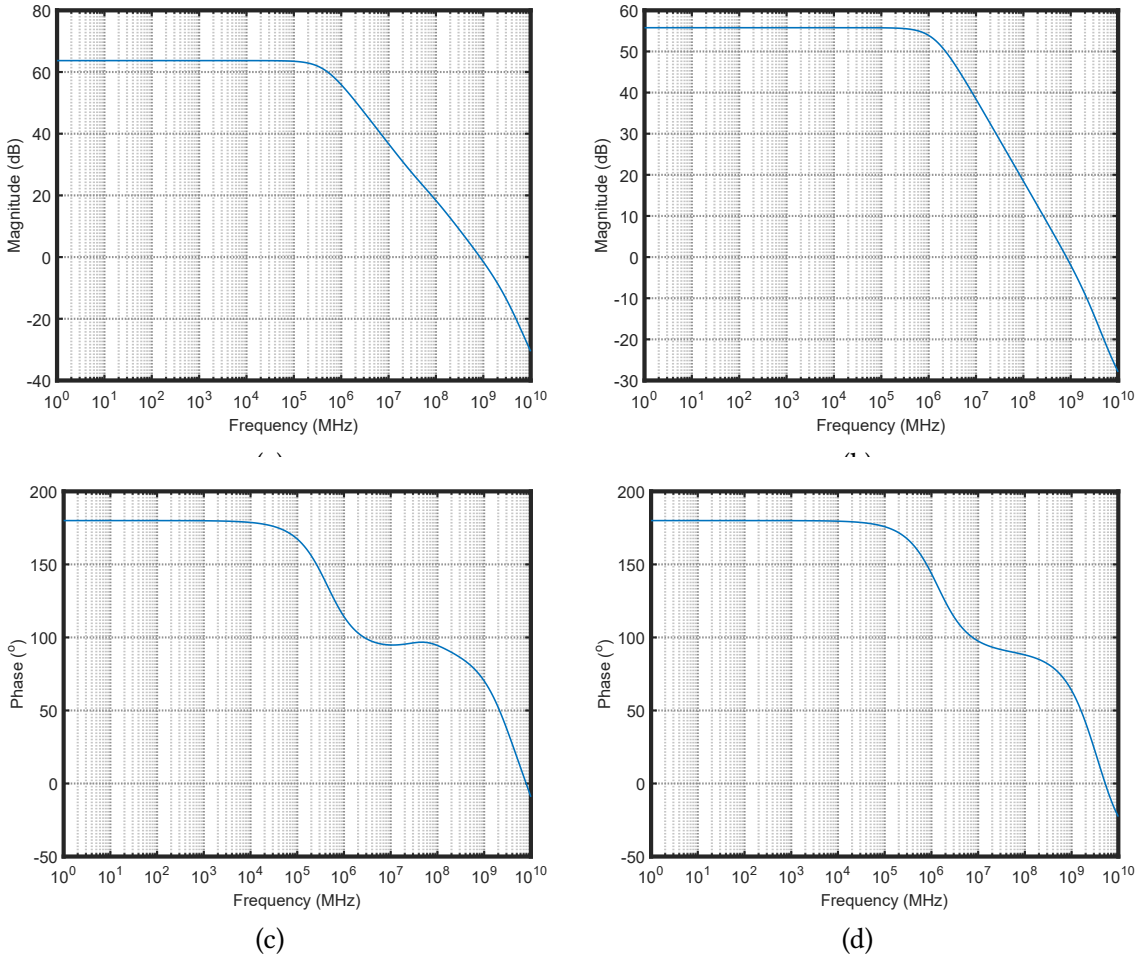


Figure 4.6: OTA frequency response in transistor-level simulations. Magnitude for the OTA with 1.2 V transistors in (a), and the OTA with 1.8 V transistors in (b); Phase for the OTA with 1.2 V transistors in (c) and for the OTA with 1.8 V transistors in (d).

(DIETRICH; HAASE, 2012). Figs. 4.8a, 4.8b and 4.8c show the process variation for DC gain, phase margin and GBW respectively. In typical conditions (TT devices, 27^{o}C and 1.8 V) the gain is 63 dB, the phase margin is 73^o and the is GBW 850 MHz. From the Monte-Carlo results it is clear that the positive feedback scheme used in the design of the amplifier (Fig. 3.7) to increase gain is, as expected, very sensitive to process variations, where the DC gain varies from 40 dB to 90 dB. For the OTA with 1.8 V transistors the gain was 56 dB, the GBW, 810 MHz, and the phase margin 68^o. A small reduction that based on macro-model simulations should not impact the ΣΔM performance. For brevity, Monte-Carlo simulations will not be displayed for this iteration, but a similar variation compared to the previous design is expected.

To verify the operational amplifier transient performance, the test-bench of Fig. 4.5b (DEHGHANI, 2013) is used to evaluate the SR and overall transient performance respectively (for the latter case the feedback resistor was doubled). To evaluate the Slew Rate, the

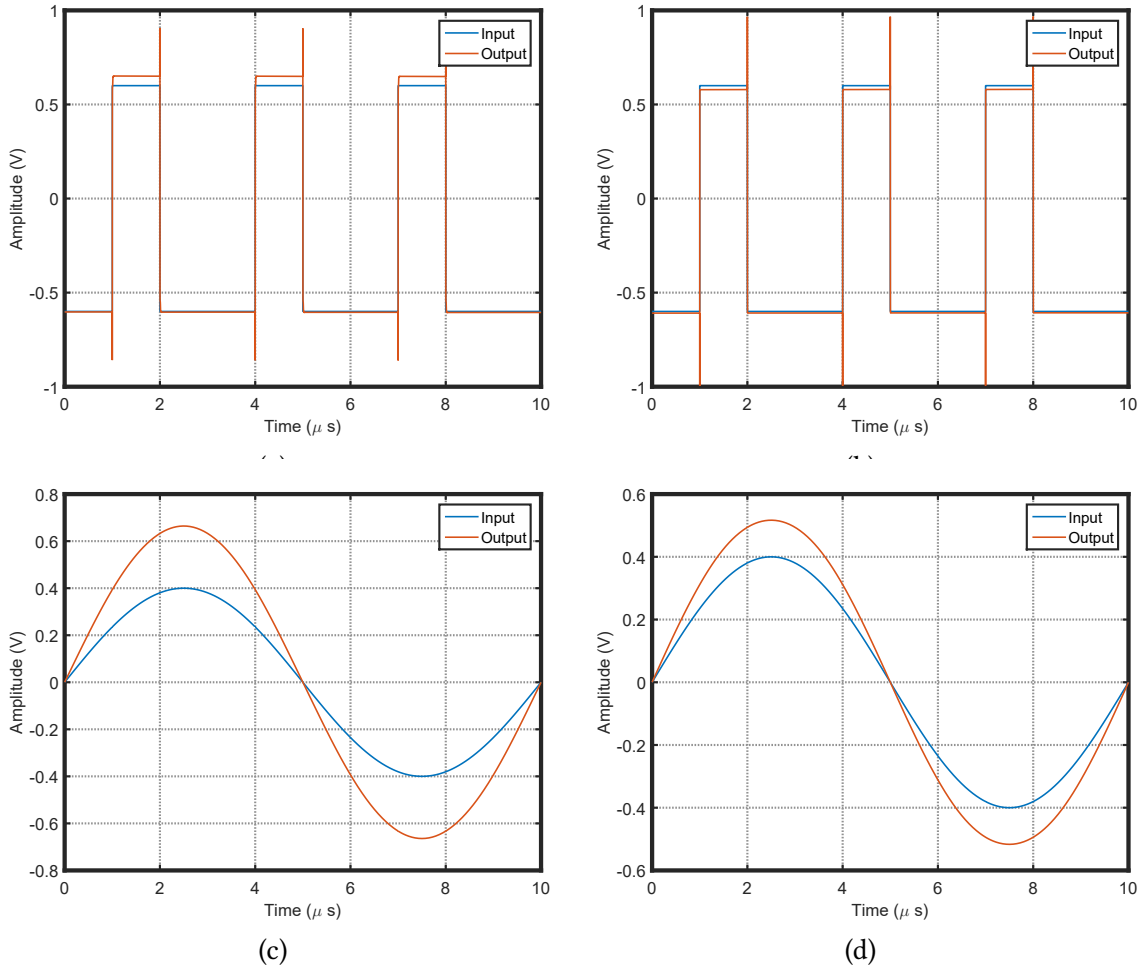
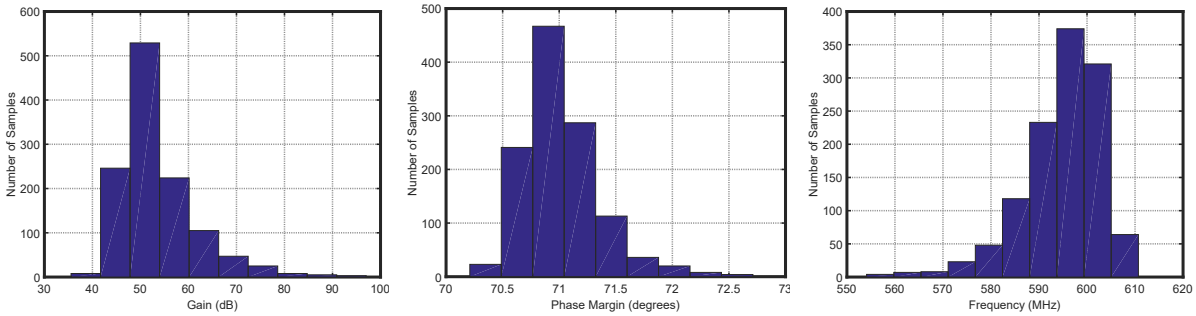


Figure 4.7: OTA transient response in transistor-level simulations. Slew Rate for the OTA with 1.2 V transistors in (a), and the OTA with 1.8 V transistors in (b); Transient with a closed loop configuration to double the gain for the OTA with 1.2 V transistors in (c) and for the OTA with 1.8 V transistors in (d).

operational amplifier is set up in a unit gain configuration with a capacitors in parallel with a large resistors to provide the necessary DC path (DEHGHANI, 2013). Then, the response to a input differential step varying from -600 to 600 mV is verified with a load capacitance of 250 fF. Fig. 4.7a presents the output waveform for the OTA with 1.2 V transistors and Fig. 4.7b, shows the results for the OTA with 1.8 V transistors. The obtained SRs are, 844 V/µs and 687 V/µs respectively. A typical transient performance is shown in Figs. 4.7c and 4.7d. It is clear that the output swing of the OTA with 1.8 V is not enough and distorts the output signal. This, alongside the reduction in SR, compared to the 1.2 V transistor implementation counterpart, was a major factor in the ΣΔM performance, as it will be shown in Section 4.2.9.

Additionally, other tests were performed in the OTA with 1.2 V transistors. Fig. 4.5c shows the test-bench to evaluate the differential DC output voltage (ROSA, 2018). A DC sweep analysis varying the input voltage V_{IN} from -1.8 to 1.8 V. Fig. 4.9a shows the obtained



(a) (b) (c)

Figure 4.8: Monte Carlo 3σ variation for mismatch and process with 1200 samples for transistor-level simulations. (a) Gain; (b) Phase Margin; (c) Gain Bandwidth.

output voltage swing varying from approximately -1.4 to 1.4 V. Fig. 4.5d presents the test-bench to evaluate the maximum output current swing and transconductance (g_m) (ROSA, 2018). Similarly to the previous test-bench, a DC sweep analysis is performed varying the input voltage and capturing the output current with DC voltage sources (V_{CM} = 900 mV) connected to the output pins of the amplifier. The transconductance is obtained by computing dI_{out}/dV_{in}. Fig. 4.9b shows the maximum output current saturating at around ±220 µA. The transconductance is shown in Fig. 4.9c with a maximum value of approximately 2 mA/V. Both OTAs performances are summarized in table 4.1.

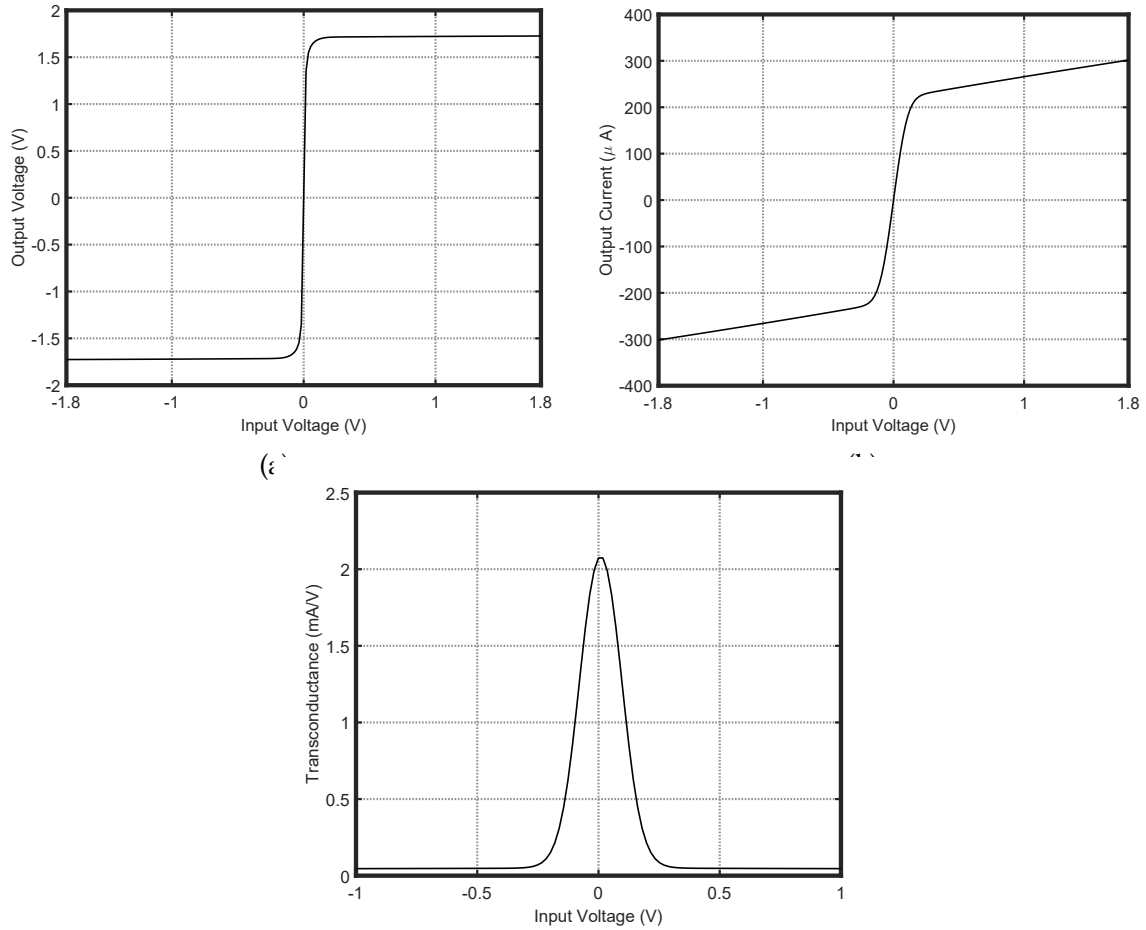
Table 4.1: Operational amplifier performance summary.

Specification	**1.2 V MOSFETs**	**1.8 V MOSFETs**
Supply (V)	1.8	1.8
GBW (MHz) C_L **= 250 fF**	850	810
DC Gain (dB)	63	56
Phase Margin (°)	73	68
Power (µW)	4.53	2.95
Slew Rate (V/µm) C_L **= 250 fF**	844	687

4.2.2 Comparators

For ΣΔM, the comparators performance is not very demanding as explained in Section 3. Main parameters measured for this project were the offset and comparison time.

For dynamic-latch-based comparators, the offset simulation evaluation (and specially fabricated chip measurement) is not simple. A few techniques exist such as the Input Ramp method and the Bisectional Method (ROSA, 2018), however the Input Ramp method,



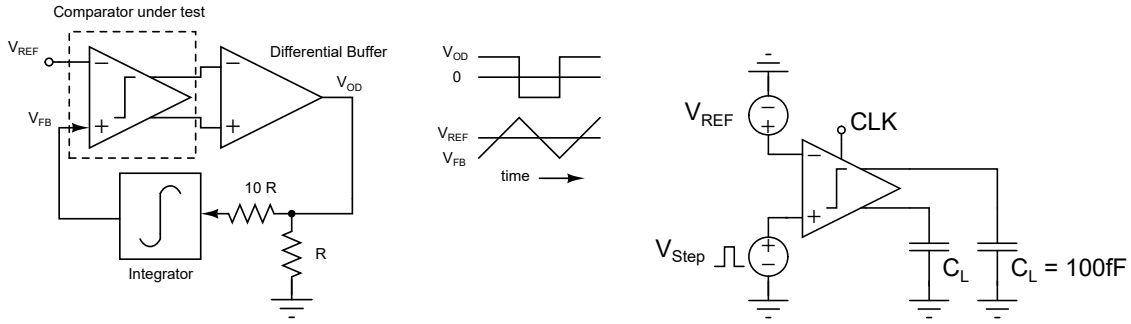
(c)

Figure 4.9: Operational amplifier DC characterization in transistor-level simulations: (a) Differential output voltage; (b) Differential output current; (c) Transconductance.

although widely used in static comparators, requires long simulation times for dynamic-latches and is not very accurate for this type of topology, while the Bisectional Method is more efficient, but requires a more complex algorithm to be performed. For these reasons the Dynamic-Offset Test-Bench (DOTB) from (MATTHEWS; HEEDLEY, 2005) was used and is depicted in Fig. 4.10a. It consists of a feedback loop where the output of the comparator goes through an integrator and is compared with a fixed DC voltage reference (V_{REF}). Since the output of the comparator is a waveform varying from -1.8 to 1.8 V, its integral is a triangular waveform that will ripple between V_{REF}. The average of the triangular waveform minus V_{REF} gives the offset value.

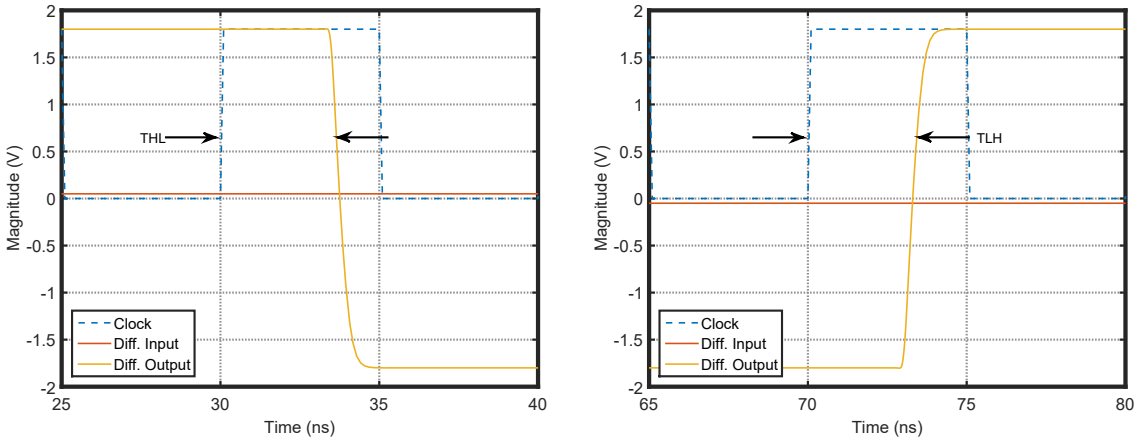
Since the offset source comes from process and mismatch variations, a Monte-Carlo analysis must be performed. The results are shown in Fig. 4.12a. Maximum offset is 9 mV.

The comparison time is measured from the test-bench of Fig. 4.10b. A small input of amplitude 50 mV is compared with 0 V and the comparison time is measured from the rising



(a) (b)

Figure 4.10: Comparator test-benches. (a) DOTB; (b) comparison time.



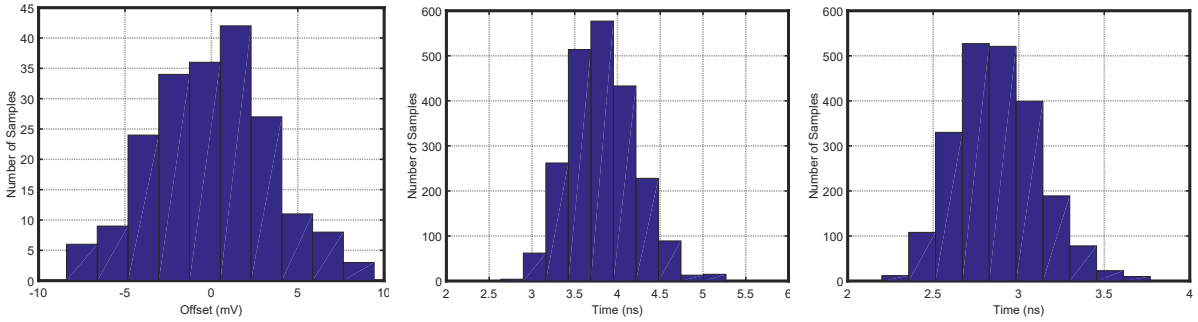
(a) (b)

Figure 4.11: Comparator comparison time transistor-level simulations. (a) Falling edge; (b) rising edge.

edge of clock to the rising or falling edge of the differential output waveform. Results for typical conditions are in Fig. 4.11 and the Monte Carlo simulations are shown in Figs. 4.12b and 4.12c for falling and rising comparison times respectively. Maximum comparison time occurs for the falling edge and is approximately 3.5 ns.

Table 4.2: Comparator performance summary.

Parameter	**Min.**	**Typ.**	**Max.**
Supply Voltage (V)	1.7	1.8	1.9
Power Consumption (µW)	-	8.73	-
Offset (mV)	-	0	9
Comparison Time (ps)	3075	3075	3273



(a) (b) (c)

Figure 4.12: Monte Carlo 3σ variation for mismatch and process in transistor-level simulations. (a) Offset (200 samples); (b) Falling comparison time (2200 samples); (c) Rising comparison time (2200) samples.

4.2.3 Multi-bit Quantizer

Fig. 4.13 presents the multi-bit quantizer transient test-bench. A transient input with amplitude of ±1 V is used, and the analog-to-digital-to-analog conversion is evaluated at the output. The analog input, output and voltage thresholds are shown in Fig. 4.14a and the digital outputs are shown in Fig. 4.14b.

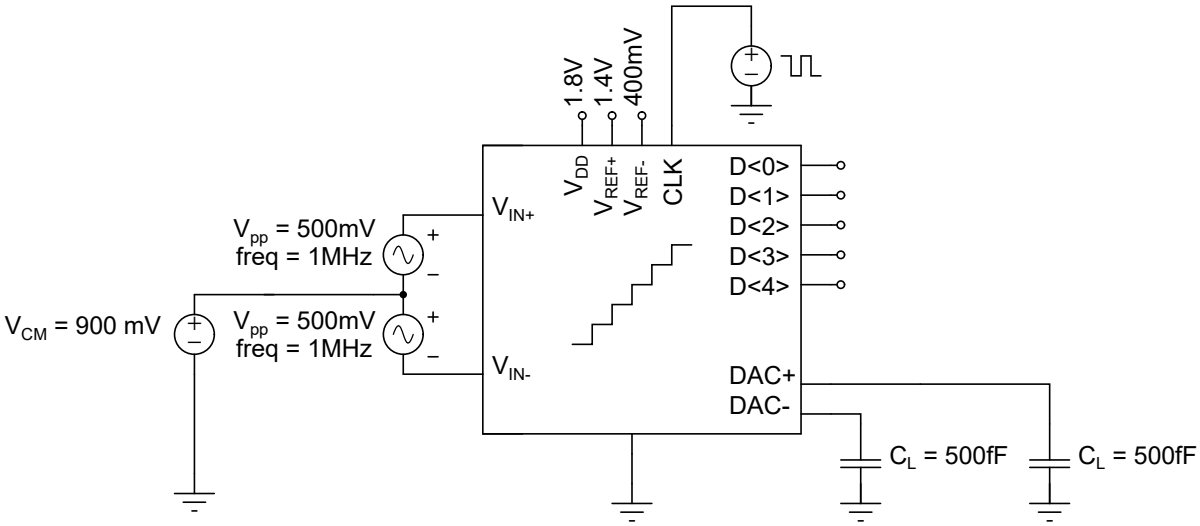
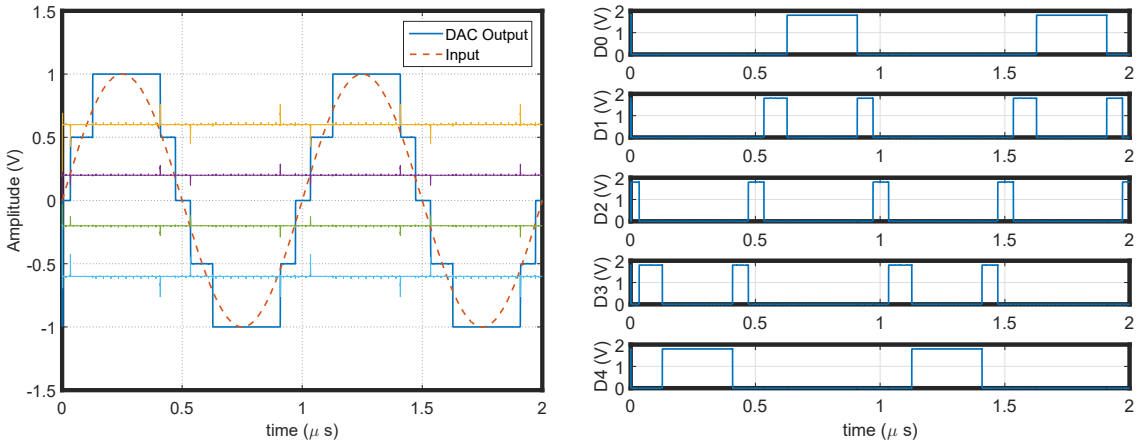


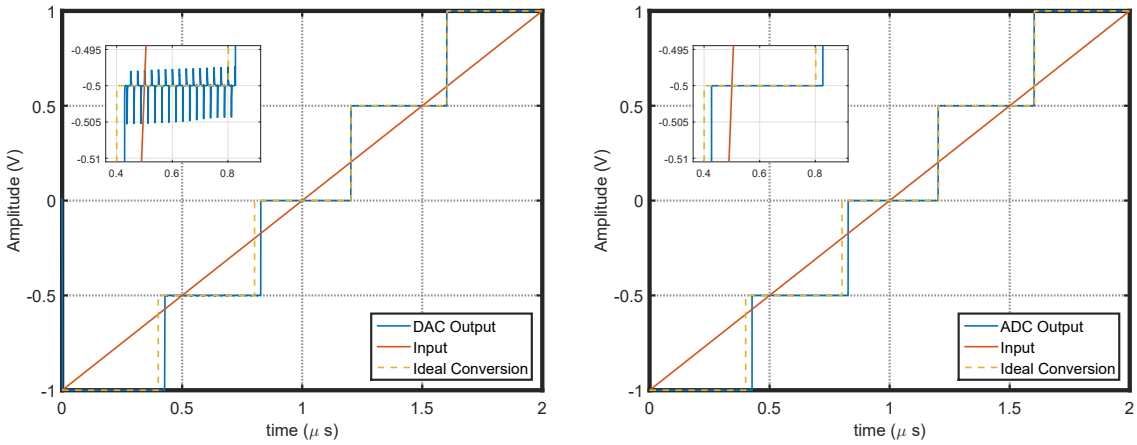
Figure 4.13: Multi-bit quantizer test-bench.

Using the same test-bench a simple measurement was performed with an input ramp and compared with an ideal DAC conversion shown in Fig. 4.15a. Fig. 4.15b shows the ADC conversion (after and ideal DAC conversion) versus an ideal conversion. The total average power consumption of the quantizer is 74.9 µW.



(a) (b)

Figure 4.14: Quantizer transient operation. (a) Analog output; (b) Digital output (transistor-level simulations).



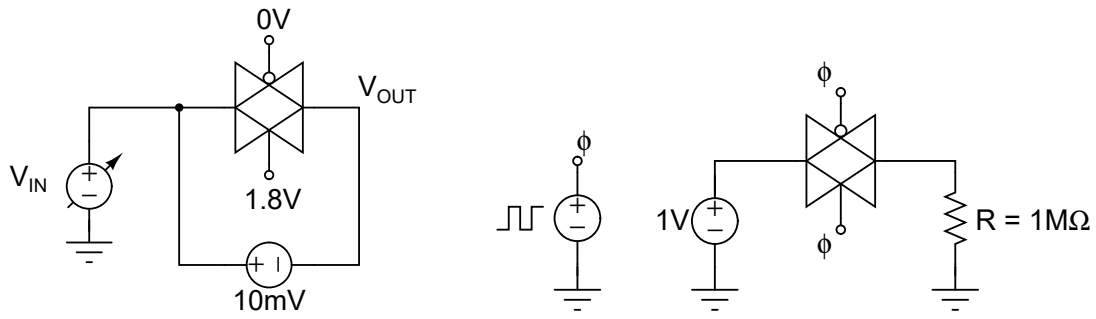
(a) (b)

Figure 4.15: Quantizer static DA and AD conversions compared to ideal conversions. (a) DAC; (b) ADC (transistor-level simulations).

4.2.4 Switches

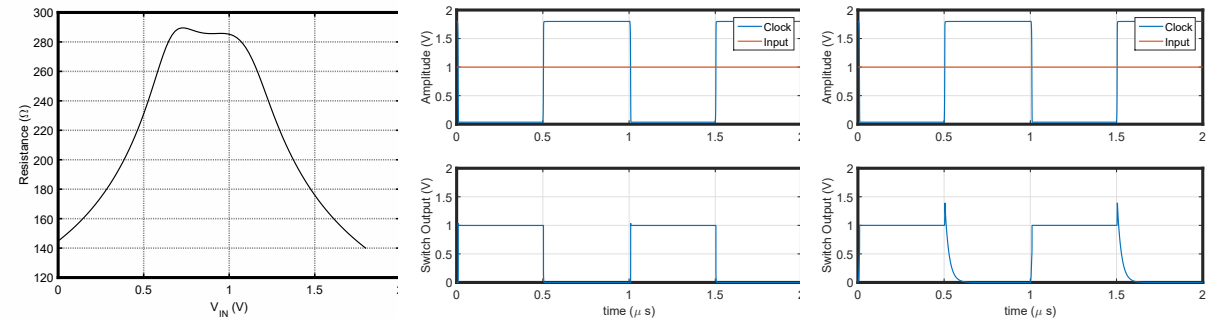
Fig. 4.16a shows the transmission gate equivalent resistance evaluation test-bench, and Fig. 4.16b presents the transient test-bench used for both the transmission gate and the input bootstrapped switch.

The on-resistance of the transmission gate is shown in Fig. 4.17a, the transient operation of the transmission gate is shown in Fig. 4.17b and the transient operation of the bootstrapped switch is shown in Fig. 4.17c. The maximum resistance is close 300 Ω and it happens when V_{in} is 900 mV. From initial transistor simulations it was verified that the bootstrapped switch used as the input switches achieve a similar SNR compared to an input transmission gate with a slightly smaller area.



(a) (b)

Figure 4.16: Switches test-benches. (a) DC; (b) transient.



(a) (b) (c)

Figure 4.17: On-resistance and transient response of the switches from transistor-level simulations. (a) Transmission gate R_{ON}; (b) Bootstrapped switch transient; (c) Transmission gate transient.

4.2.5 PLL-Based Clock Synthesizer

All simulations for the Clock Synthesizer were performed in an extracted layout view, including parasitics and corners for process, supply variation and temperature. The PLL design was realized in TSMC 65 nm process with a supply voltage of 1.2 V. For the LF, Metal-Oxide-Metal (MoM) capacitors were used, while for the resistor, Poly-Resistors were used. Fig. 4.18 shows the transient simulation test-bench, where all the following results were obtained. Complete layout is presented in Fig. 4.3.

Figs. 4.19a to 4.19f show the obtained spectrum for the selected frequencies of 40, 60 and 80 MHz in Typical-Typical (TT) conditions (TT devices, supply at 1.2 V and 27°C) and worst case condition (FF devices, supply at 1.3 V and $80^0 C$) respectively, spanning between 100 MHz and 300 MHz. The spectrum showed an expected degradation as devices tend to fall in the Fast-Fast (FF) process variation, mostly caused by variations in the CP current, VCO gain and LF resistances and capacitances, which in turn alter the PLL transfer function.

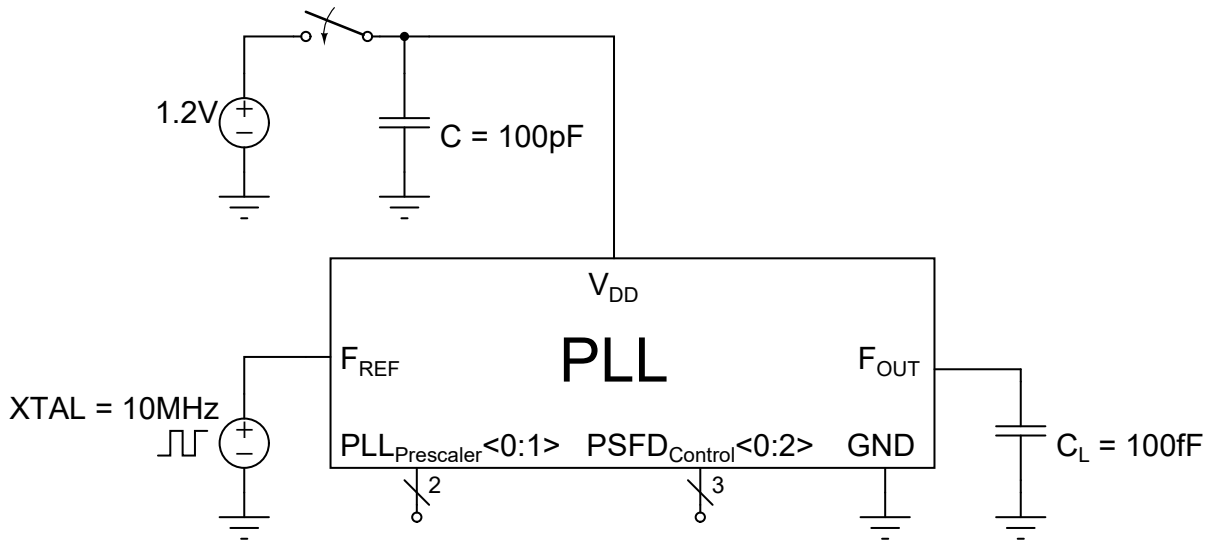
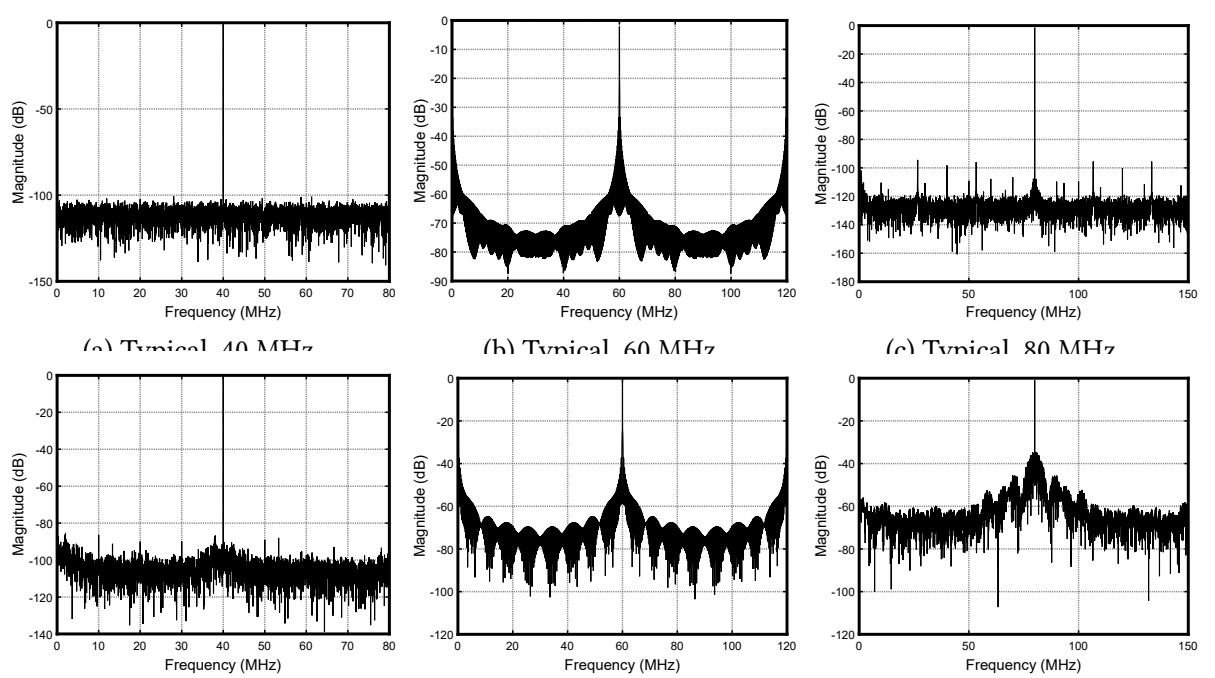


Figure 4.18: PLL test-bench.

Table 4.3: Performance summary of the clock synthesizer from extracted layout simulations after PVT corners.

Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Supply Voltage	1.1	1.2	1.3	V
Avg. Dynamic Power	299	385	634	µW
Frequency Tuning Range	40	-	230	MHz
KVCO	156.8	198.4	198.5	MHz/V
Settling Time	3.7	4	6	µs
Jitter	-	0.17	2.01	ns
Maximum Spur	-	-70	-47	dB
Area	114x324 (0.037)			µm (mm^2)

Jitter response was obtained via the eye diagram plot performed in Cadence Virtuoso environment, shown in Fig. 4.20. As expected from the spectra, jitter showed to be worst in FF, 1.3 V supply voltage and 80^{o}C condition for the 80 MHz frequency, resulting in 1.6 ns. For typical conditions the jitter is 15 ps, 1.5 ns and 21 ps for 40, 60 and 80 MHz respectively. In worst case conditions the jitter increases to approximately 1.6 ns for all cases. The discrepancy for 60 MHz is due to the 50 % duty cycle divide-by-3 circuit at the output of the PLL which adds a lot of jitter. Another test was performed with a less jittery divide-by-3 circuit with a 33-66% duty cycle, however the results integrated with the ΣΔM were worse than with the previous divider. A solution to this problem would be the use of the 57.5 MHz frequency that is originated from the divide-by-4 output which adds much less jitter.



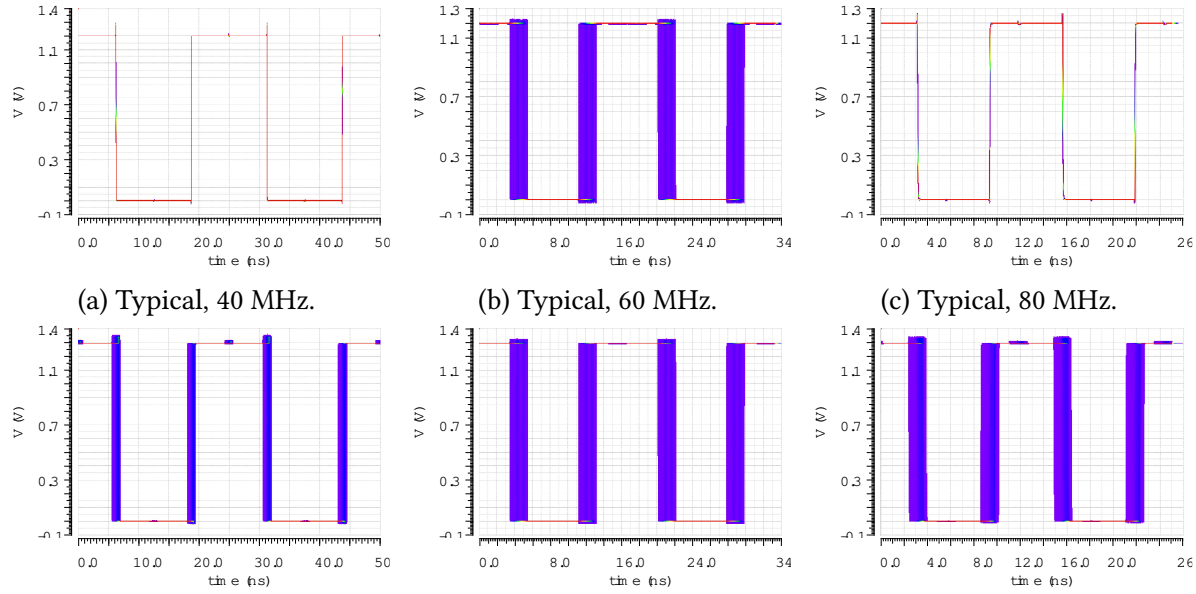
(a) Typical, 40 MHz (b) Typical, 60 MHz (c) Typical, 80 MHz

(d) Worst case, 40 MHz (e) Worst case, 60 MHz (f) Worst case, 80 MHz.

Figure 4.19: Clock synthesizer spectra for main frequencies. Typical: 1.2 V, 27 ^{o}C, TT; Worst case: 1.3 V, 80 ^{o}C, FF (obtained from extracted layout simulations).

These simulations only capture the deterministic portion of the total jitter, however this verification is a sufficient preliminary result to give an idea of the PLL behavior in worst case conditions. Several jitter and duty cycle correction circuits have been reported (ROMANO et al., 2002), (WU et al., 2009), (YUN CHEN; CHAOJIE FAN; JIANJUN ZHOU, 2013) and can be used alongside calibration techniques to improve performance in worst corners. For future iterations of this design, where the target application requires less jitter, the ideal solution is a system-level change in the PLL, starting with the VCO, which would improve the phase noise dramatically compared to the inverter-based ring oscillator.

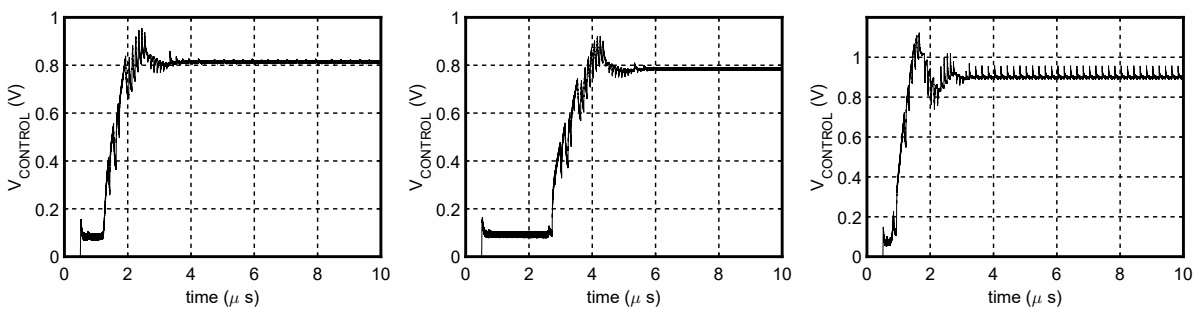
Fig. 4.21 presents the settling behavior of the control voltage fed to the VCO when 200 MHz is selected. Worst case condition in this parameter is specifically for total settling time, which happens with Slow-Slow (SS) devices at 0^{o}C and with supply at 1.1 V resulting in total settling time of about 6 µs. Although the worst case results in worst settling time, the ripple in settled condition is actually smaller than typical operation, resulting in a cleaner spectrum, and less jitter, which is desirable for the proposed application since there are no strict requirements in regards to settling time. Fig. 4.22 shows the settling behavior for every selectable output frequency (before the output division).



(a) Typical, 40 MHz. (b) Typical, 60 MHz. (c) Typical, 80 MHz.

(d) Worst case, 40 MHz (e) Worst case, 60 MHz (f) Worst case, 80 MHz.

Figure 4.20: Clock synthesizer eye diagram for main frequencies. Typical: 1.2 V, 27 ^{o}C, TT; Worst case: 1.3 V, 80 ^{o}C, FF (obtained from extracted layout simulations).



(a) (b) (c)

Figure 4.21: Control voltage when 200 MHz is selected for (a) TT, 27 ^{o}C, 1.2 V supply, (b) SS, 0 ^{o}C, 1.1 V supply, (c) FF, 80 ^{o}C, 1.3 V supply (obtained from extracted layout simulations).

The generated clock waveforms for 40, 60 and 80 MHz are shown in Fig. 4.23a, b and c respectively. Due to extremely long simulation times Monte Carlo analysis was not performed for the PLL. Performance summary of the PLL is presented in table 4.3 and comparison with other works with similar specifications is shown in table 4.4. It is clear that compared with other works, this design trades power dissipation for jitter degradation. Overall from the requirements defined in table 3.1 the PLL performance is sufficient for the proposed modulator frequencies even in worst case operation with low power consumption and small area.

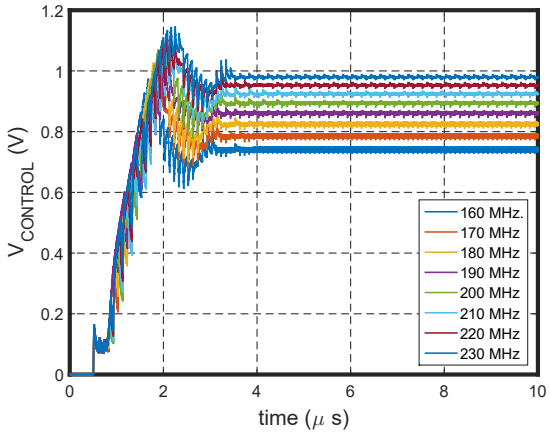
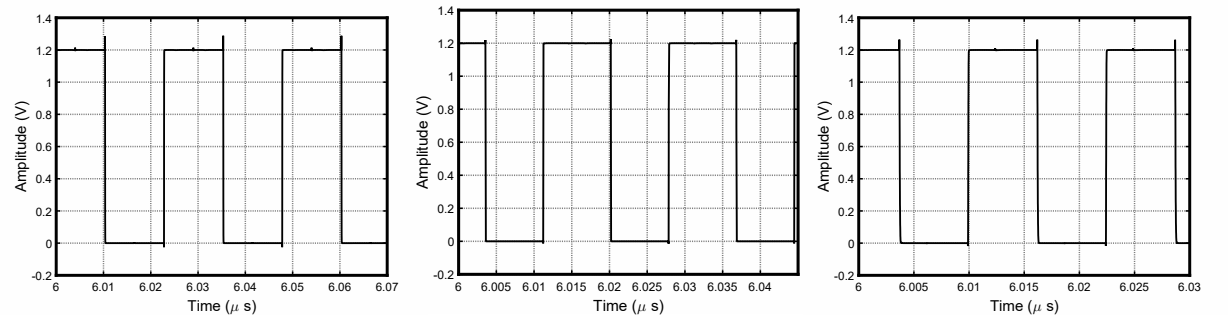


Figure 4.22: Control voltage comparison for all frequency selections, varying from 160 MHz to 230 MHz obtained from extracted layout simulations.



(a) (b) (c)

Figure 4.23: Generated clock waveform obtained from extracted layout simulations (a) 40 MHz, (b) 60 MHz, (c) 80 MHz.

Table 4.4: Comparison with other works.

	This Work	(AKIHIDE SAI et al., 2008)	(WILLIAMS et al., 2004)	(SHI et al., 2006)
Ref. Freq. (MHz)	10	20	27	20
Nom. Freq. (MHz)	200	200	270	350
Tech. (µm)	0.65	0.9	0.35	0.18
Supply (V)	1.2	1.2	1.8	3.3
Area (mm^2)	0.037	0.18	0.09	0.16
Power (mW)	0.385	9	12	24
Jitter (ps)	170	3	7.1	4

PLL Measurement

For the PLL, initial measurements were also performed on the fabricated prototype, such as the phase noise and frequency sweep range.

The measurement setup is shown in Fig. 4.24 and a diagram of the setup is shown in Fig. 4.25 for clarity. The chip incorporates a I2C interface for the digital control of the PLL, controlled by a Raspberry Pi. Both the phase noise and rms jitter are measured in the signal analyzer Keysight N9010B with 50 Ω probes. Output frequency is measured via the digital signal analyzer Agilent 91604A also using 50 Ω probes.

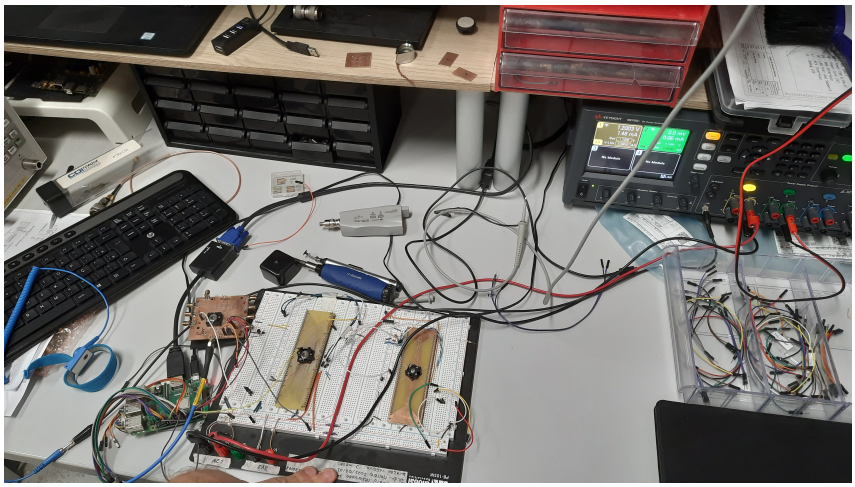


Figure 4.24: Measurement setup for the PLL.

Fig. 4.26 shows the phase noise spectrum from 1Hz to 100 MHz for a frequency output of 200 MHz. The rms jitter can be computed as the integral of the phase noise spectrum between two frequency offsets (4.1) (RAZAVI, 2020)

$$J_{rms} = \sqrt{\int_a^b S_{\phi n}(f)df}, \tag{4.1}$$

where $S_{\phi n}(f)$ is the spectrum of the phase noise, a is the upper frequency offset and b is the lower frequency offset. This measurement is made by the signal analyzer, by setting both frequency bounds. The measured rms jitter from 1 Hz to 1 MHz is 46.32 ps, and measuring from 1 kHz to 1 MHz, is equal to 1.97 ps. The phase noise at a 100 Hz offset is -84 dBc/Hz and the far out phase noise at 1 MHz is -115 dBc. There is a spurious component at 60 Hz offset that seems to be caused by a poor isolation between the supply source and the electrical network. Further measurements must be made using external regulators with better power supply rejection.

Total current drawn from the power supply is equal to 1.46 mA when the output frequency of the PLL is set to 200 MHz. The measurement includes the core of clock synthesizer, output buffers and the I2C interface. The difference from simulated results in

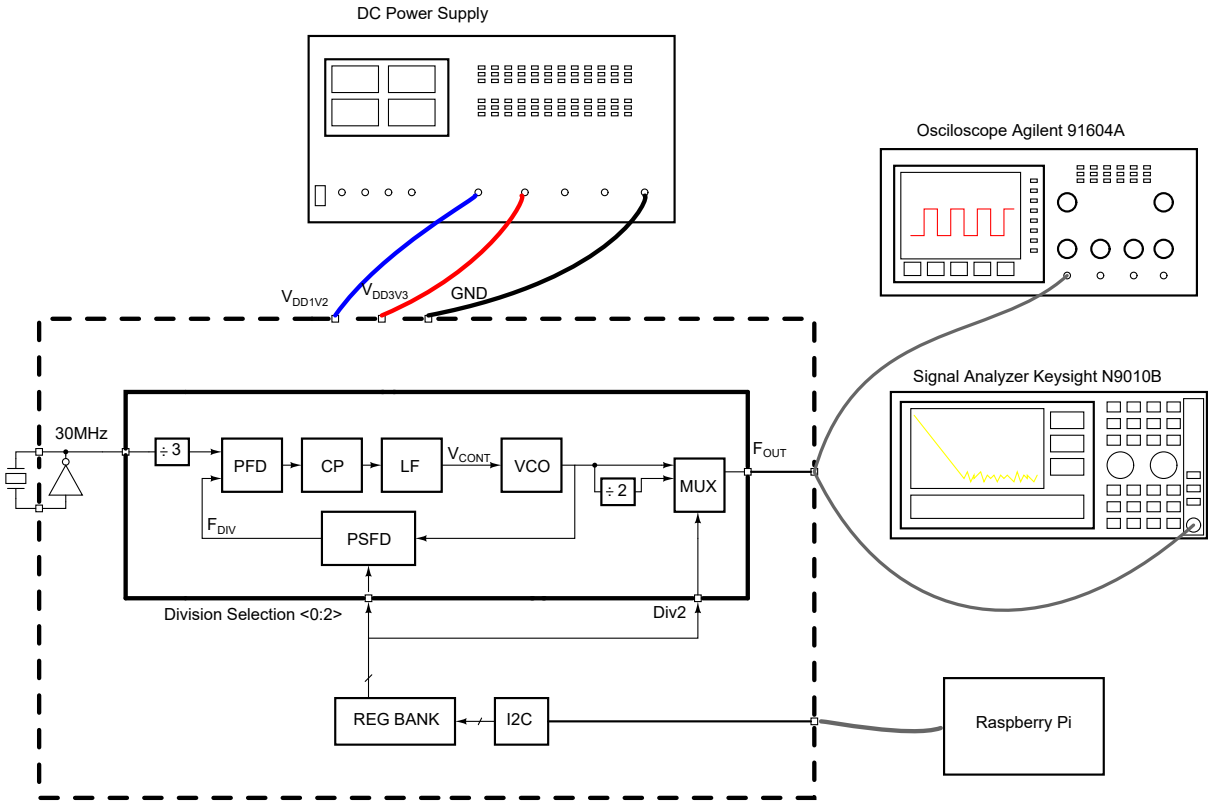


Figure 4.25: PLL measurement setup diagram.

regards to power consumption, comes from the inclusion of output buffers and the digital circuitry.

Table 4.5 shows the measured output frequencies depending on the division selection. As expected, the PLL locks for every case, and the output frequency is always the reference, multiplied by the division selection ($F_{OUT} = F_{REF} \times N$).

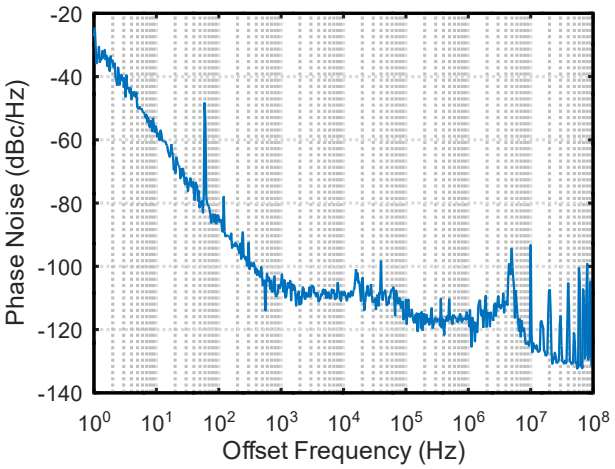


Figure 4.26: Measured phase noise spectrum of the fabricated PLL prototype.

Table 4.5: Frequency sweep measurement of the PLL prototype.

Division Selection (N)	Output Frequency (MHz)
16	160
17	170
18	180
19	190
20	200
21	210
22	220
23	230

4.2.6 Charge Pump

Fig. 4.27a presents the DC CP test-bench, and Fig. 4.27b shows the transient test-bench. The DC analysis performs a sweep in the output voltage to evaluate the up and down currents mismatch for different output voltages. Ideally V_X does not provide any current, and the worse deviation from the fixed CP current, the worst it will be for the PLL operation (with jitter an phase noise increase) (RAZAVI, 2020). The transient operation just verifies the correct CP operation.

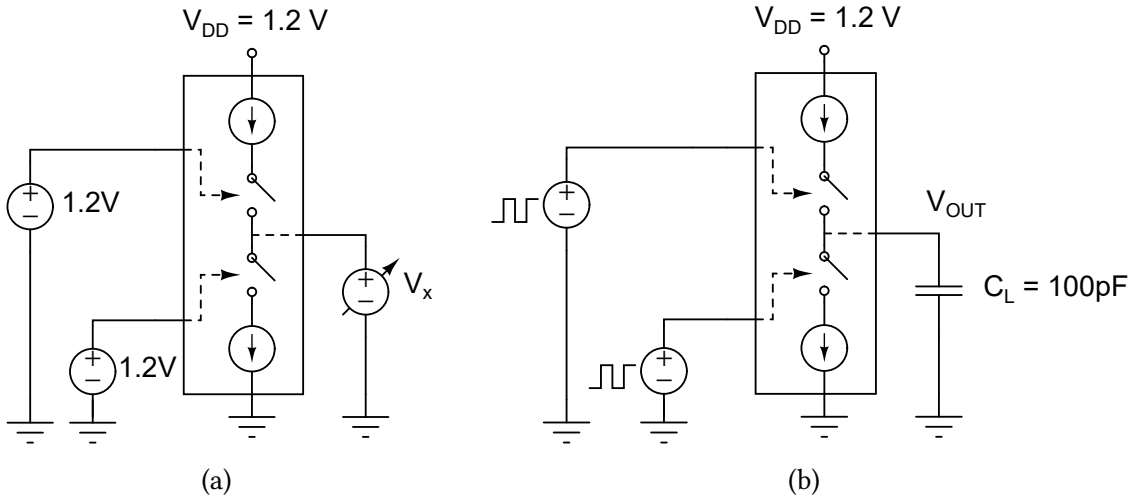
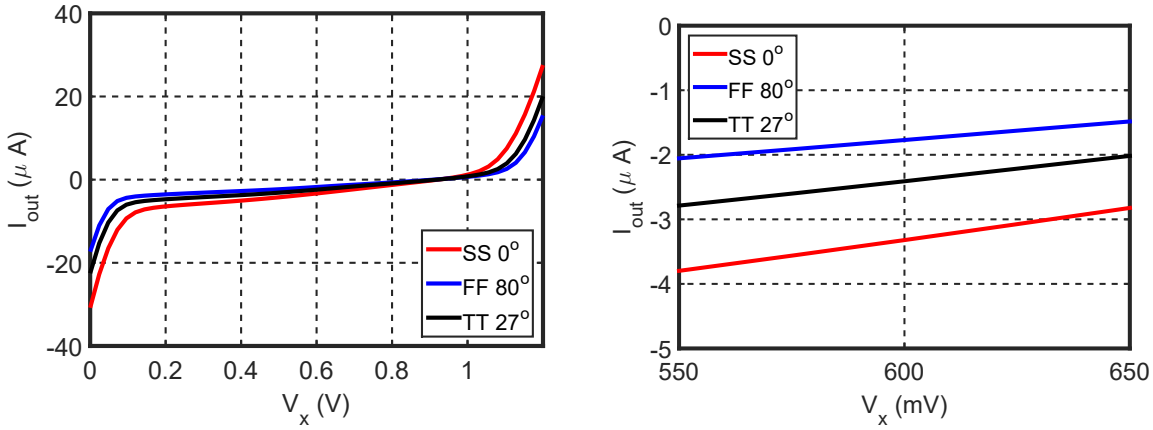


Figure 4.27: Charge Pump test-benches. (a) DC; (b) transient.

Figs. 4.28 shows the imbalance between the UP and DOWN currents for different corners. For the most part of the DC sweep, $I_{UP} > I_{DOWN}$, however, the imbalance is not severe, and does not impact the PLL operation. However, when the control voltage is higher than $1.1V$, the imbalance becomes more severe, and the settling operation of the PLL is affected. The



(a) (b)

Figure 4.28: (a) Charge Pump mismatch between UP and DOWN currents. (b) approximation of (a) between 550 mV and 650 mV (extracted layout simulations).

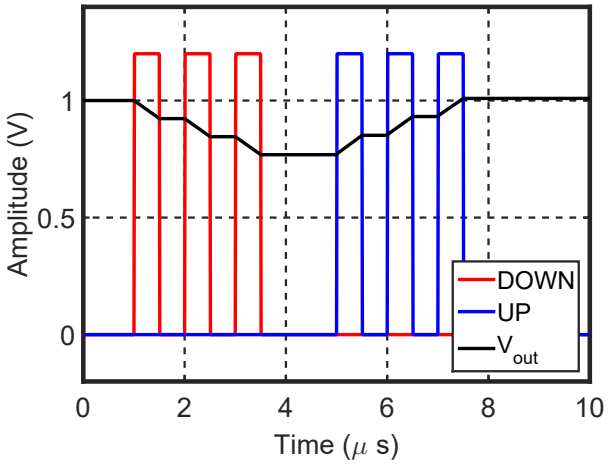


Figure 4.29: CP transient operation (extracted layout simulations).

obtained imbalance is expected and large transistors were used in the CP current mirrors to improve results. Fig. 4.29 shows the transient operation of the charge pump in worst case condition (SS, 0 ^{o}C, 1.1 V) for simple functional verification. As expected when the UP signal is HIGH, the output voltage increases and when the DOWN signal is HIGH the output voltage decreases.

4.2.7 Voltage Controlled Oscillator

Fig. 4.30 shows the VCO test-bench. A DC control voltage source is used to emulate the control voltage and a DC sweep is performed to verify the VCO frequency tuning range.

KVCO gain for extracted results for typical conditions and worst corners (SS, 0 ^{o}C, 1.1 V and FF, 80 ^{o}, 1.3 V) is shown in Fig. 4.31a. A comparison with transistor-level schematic

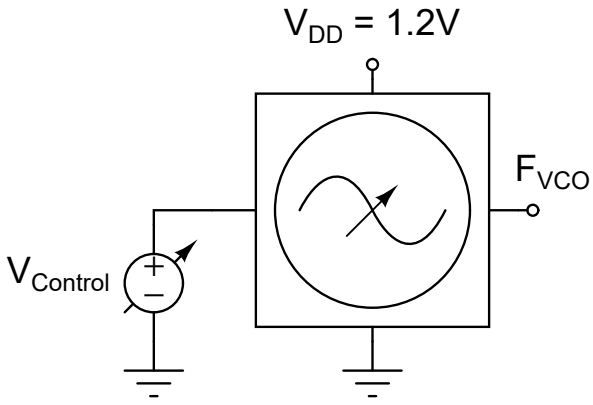
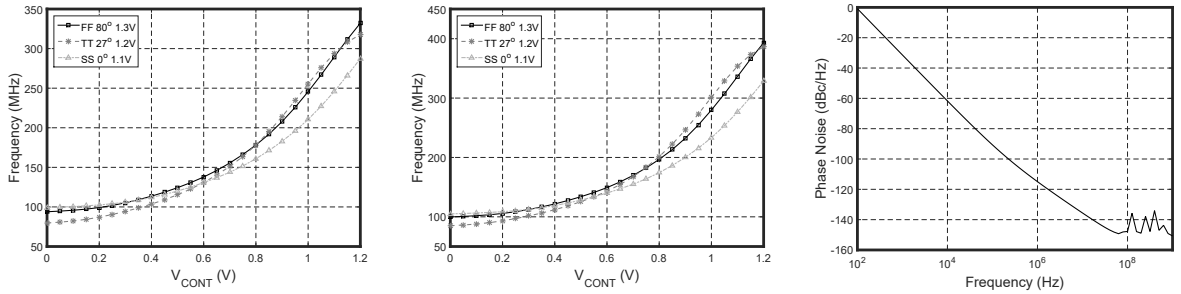


Figure 4.30: VCO test-bench.



(a) (b) (b)

Figure 4.31: (a) VCO tunning range from post-layout simulation and (b) transistor-level, and (c) phase noise for worst case condition (extracted simulation).

results is made in Fig. 4.31b to exemplify the frequency gain curve degradation due to layout parasitics.

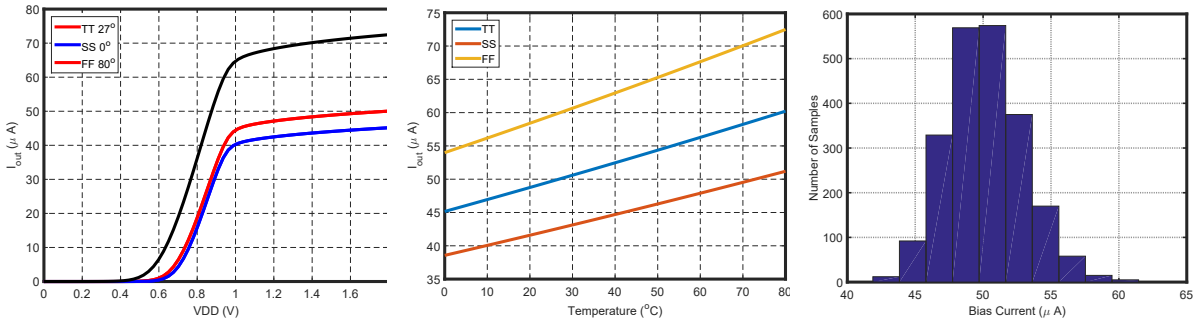
Phase noise results are presented in Fig. 4.31c. The results were the expected for this type of topology. A small improvement in phase noise characteristic can be obtained in exchange of more power consumption by the inverters (increase in W/L) (RAZAVI, 2020).

4.2.8 Auxiliary Blocks

ΣΔM Master Bias

Voltage supply sweep varying from 0 to 1.8 V is shown in Fig. 4.32a for main corners, temperature sweep is shown in Fig. 4.32b for different process variations and Monte Carlo variation with 2200 samples is shown in Fig. 4.32. The results for the master bias current generator for the ΣΔM are summarized in table 4.6. Power consumption is evaluated when all of the operational amplifier bias currents are active and the Line Regulation (LR) is measured from 1.1 to 1.3 V. The variations for supply, temperature and process are the

expected results for the topology presented in Fig. 3.23: good LR with poor Temperature Coefficient (TC) and process variation.



(a) (b) (c)

Figure 4.32: Bias currents transistor level simulation results: (a) DC sweep, (b) Temperature sweep and (c) Monte Carlo process and mismatch variation.

Table 4.6: ΣΔM master bias performance summary.

Parameter	**Min.**	**Typ.**	**Max.**
Supply Voltage (V)	1.7	1.8	1.9
Power Consumption (µW)	154.1	169.8	245.1
Output Current (µA)	45.3	50	72
Temperature Coefficient (ppm/^{o}C)	3019	3133	3920
Line Regulation (%/V)	15.5	18	19

The Temperature coefficient is defined by (4.2):

$$TC = \frac{I_{MAX} - I_{MIN}}{I_{TYP}(T_{MAX} - T_{MIN})} \times 10^6 \text{ (ppm/)}^o\text{C} \tag{4.2}$$

and Line Regulation is defined by (4.3):

$$LR = \frac{\Delta I_{out}/I_{out} \times 100\%}{\Delta I_{in}} \text{ (\%/V)}. \tag{4.3}$$

PLL Charge Pump Current

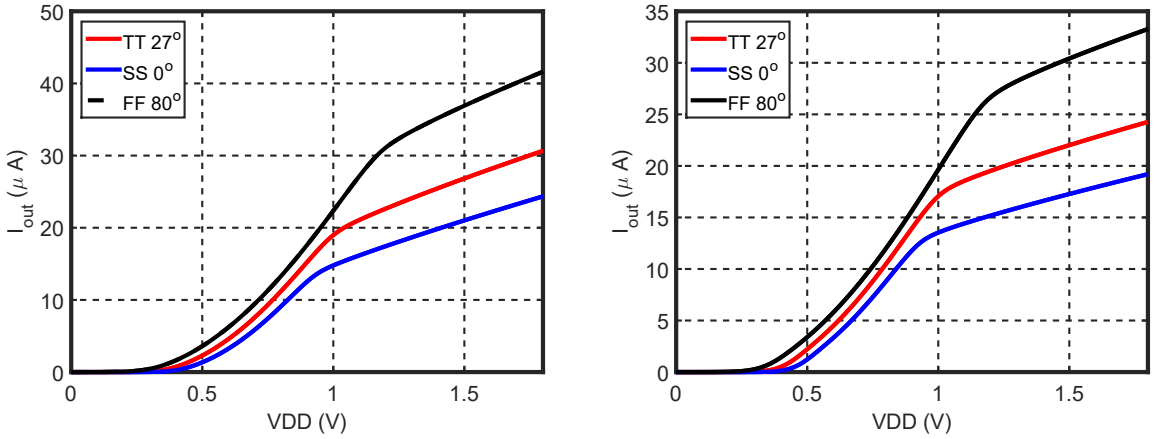


Figure 4.33: DC sweep extracted simulation results for process and temperature corners for (a) P Bias current (UP current) and (b) N bias current (DOWN current).

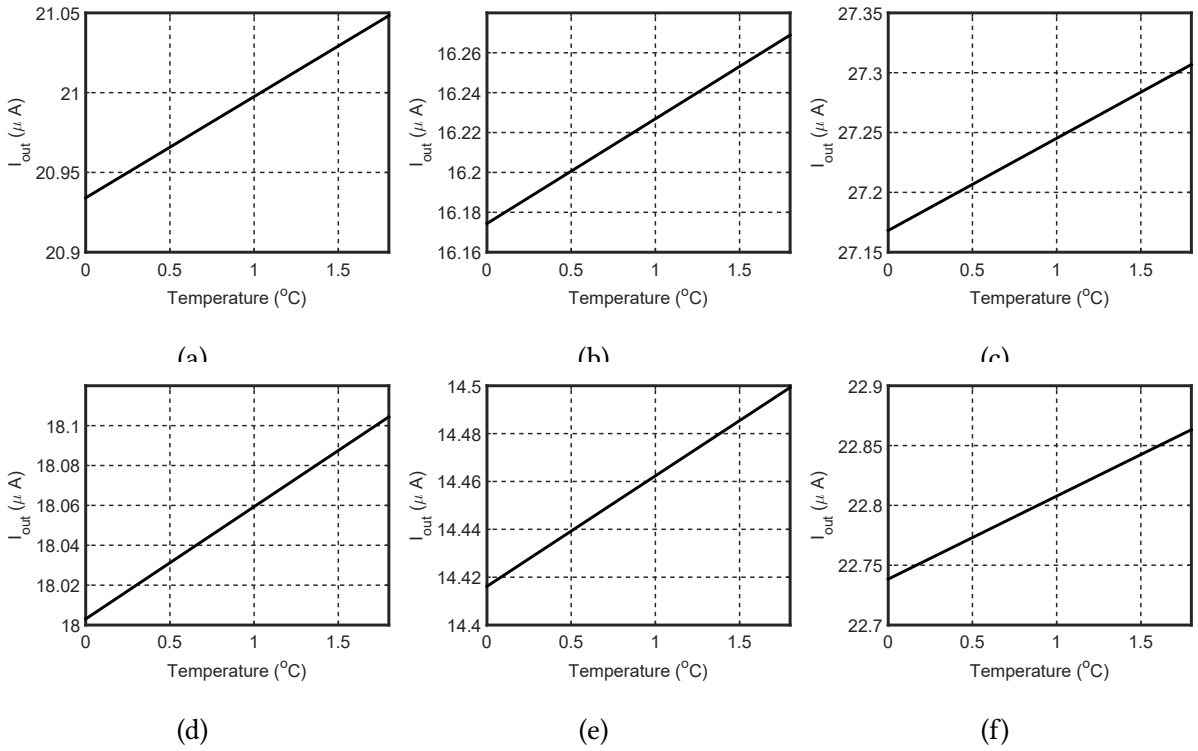
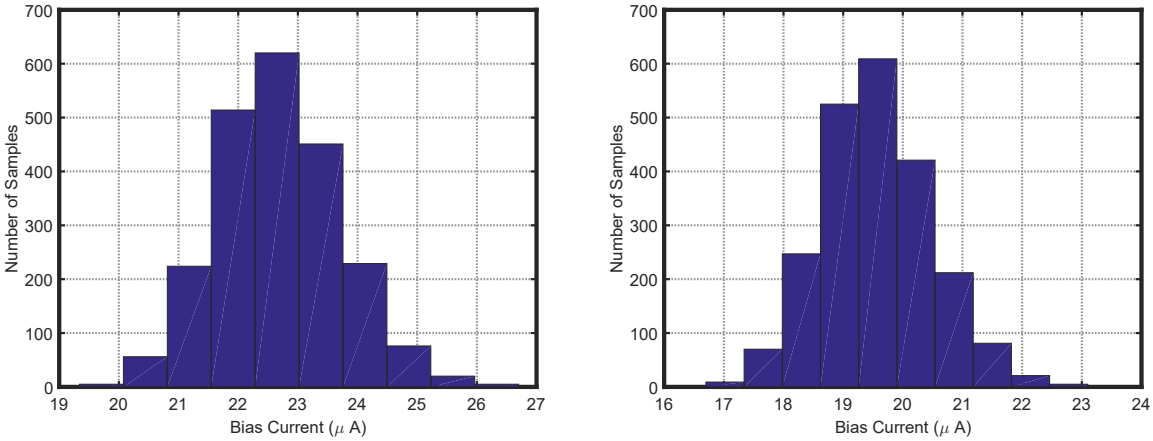


Figure 4.34: Extracted simulation results in a temperature sweep for P Bias current (UP current) for (a) TT, 1.2 V supply, (b) SS, 1.1 V supply, (c) FF, 1.3 V supply and N Bias current (DOWN current) for (d) TT, 1.2 V supply, (e) SS, 1.1 V supply, (f) FF, 1.3 V supply.

The voltage supply sweep varying from 0 to 1.8 V for main corners for both P bias (UP current) and N bias (DOWN current) are shown in Fig. 4.33. Temperature sweep for both currents

in main corners is presented in Fig. 4.34. Monte Carlo variation for 2200 samples was also performed and the results are shown in Fig. 4.35.

Table 4.7 summarizes the current source performance.



(a) (b)

Figure 4.35: Extracted simulation results for Monte Carlo 3 σ process variation with 2200 samples for (a) P bias current and (b) N bias current.

Table 4.7: CP Current source performance summary.

Parameter	**Min.**	**Typ.**	**Max.**
Supply Voltage (V)	1.1	1.2	1.3
Power Consumption (μW)	38.4	50.4	67.2
Output P Current (μA)	16	21	28
Output N Current (μA)	14.4	18.1	23
Temperature Coefficient (ppm/^{o}C)	2587	2587	4461
Line Regulation (%/V)	21	47	95

4.2.9 Complete Modulator Simulation Results

Fig. 4.36 shows the ΣΔM transient simulation test-bench. The results highlighted in this section compromise of 6 simulation configurations: 1) simulations using Verilog-A models in the sub-blocks of the ΣΔM with ideal clocks; 2) replacing the ideal clock from the previous scheme to the PLL-generated clock; 3) Transistor simulation of the ΣΔM with ideal clocks using OTAs with 1.2 V transistors, 4) transistor simulation of the ΣΔM using OTAs with 1.2 V transistors with PLL-generated clocks, 5) Transistor simulation of the ΣΔM with ideal clocks using OTAs with 1.8 V transistors, 6) transistor simulation of the ΣΔM using OTAs with 1.8 V transistors with PLL-generated clocks.

From these results conclusion can be reached in relation to the degradation of the modulators performance with the use of real clocks, the transistor implementation and difference between the OTAs with 1.2 and 1.8 V transistors.

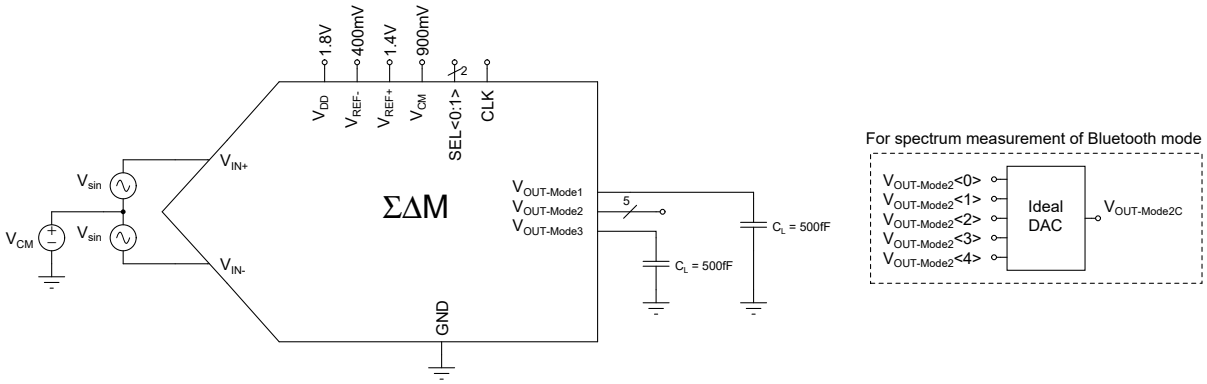


Figure 4.36: ΣΔM test-bench.

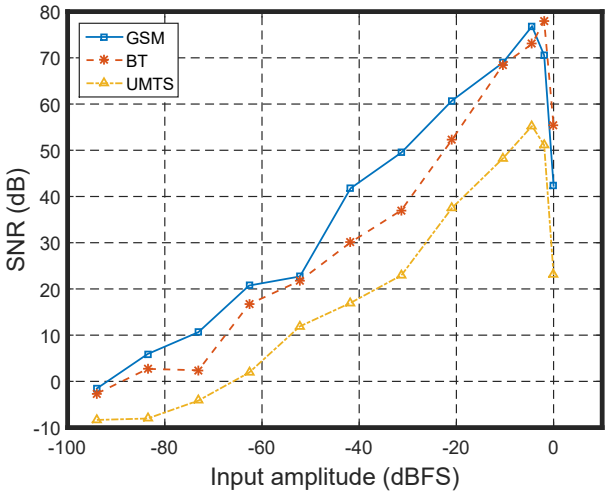


Figure 4.37: SNR with input amplitude variation for each mode obtained from macro-model simulations.

The SNR versus the input signal amplitude is plotted in Fig. 4.37 for every operation mode with ideal clocks to evaluate optimal performance. Peak performance is obtained at around -4 dBFS for GSM and UMTS, and -3 dBFS for BT, where the value in dBFS is given by (4.4)

$$Value\ (dBFS) = 20log\left(\frac{|V_{in}(V)|}{V_{FS}(V)}\right), \tag{4.4}$$

where V_{in} is the input amplitude and V_{FS} is the full scale range of 1 V. For values above -2 dBFS, the modulator becomes unstable and the SNR starts to drop sharply.

Figs. 4.38, 4.39 and 4.40 shows the power spectrum density of the proposed modulator for all modes of operation GSM (BW = 200 kHz), BT (BW = 500 kHz) and UMTS (BW = 2 MHz)

considering ideal and PLL-generated clocks for: 1) macro-model simulations, 2) transistor-level simulation using OTAs with 1.2 V transistors, and 3) transistor-level simulation using OTAs with 1.8 V transistors respectively. All spectra use a sinusoidal input waveform with amplitude of approximately -4 dBFS. Results were taken using 8192 samples in the FFT with Hanning window and coherent sampling (RENESAS, 1999). The input frequency for the GSM case is 53 kHz, for the Bluetooth mode is 124 kHz, and for the UMTS case, 166 kHz. Table 4.8 summarizes the proposed modulator performance for each mode of operation.

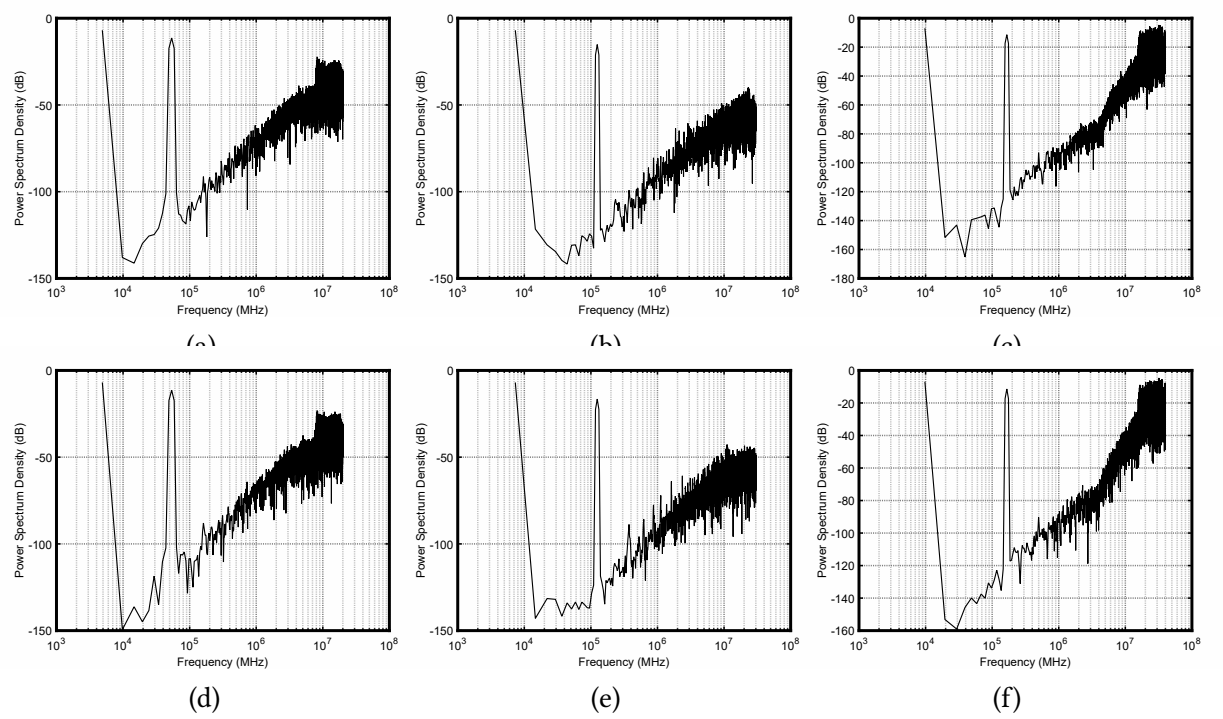


Figure 4.38: Power Spectrum Density for each mode of operation (Hanning Window with 8192 FFT points). Macro-model results with ideal clocks for (a) 40, (b) 60 and (c) 80 MHz; Macro-model results with PLL-generated clock for (d) 40, (e) 60 and (f) 80 MHz.

Overall main performance specifications defined by table 3.1 (also reproduced in table 4.8) were met for GSM and UMTS using the OTAs with 1.2 V transistors. The modulator achieved an Effective Number of Bits of 11.51 for GSM operation and 8.82 bits for UMTS with ideal clocks compared to 12.15 and 8.94 from macro-model simulations. For Bluetooth operation the degradation was more severe during circuit integration, achieving 10.16 bits compared to 12.31 in the Verilog-A implementation. When PLL generated clocks are used the results are 11.56, 9.87 and 8.63 for GSM, BT and UMTS respectively. A small improvement for GSM and UMTS compared to the ideal clock case, and a further deterioration for Bluetooth.

Third harmonic spurious components were presented in a few of the obtained spectra after transistor integration. From comparison with macro-model simulations, major contributors to

the increase of the third harmonic in the spectra would be the capacitive coupling of the CMOS switches and resistance non-linearity, the limited Slew-Rate and DC gain of the operational amplifier. The dynamic range is highlighted by the Spurious Free Dynamic Range (SFDR) parameter of table 4.8.

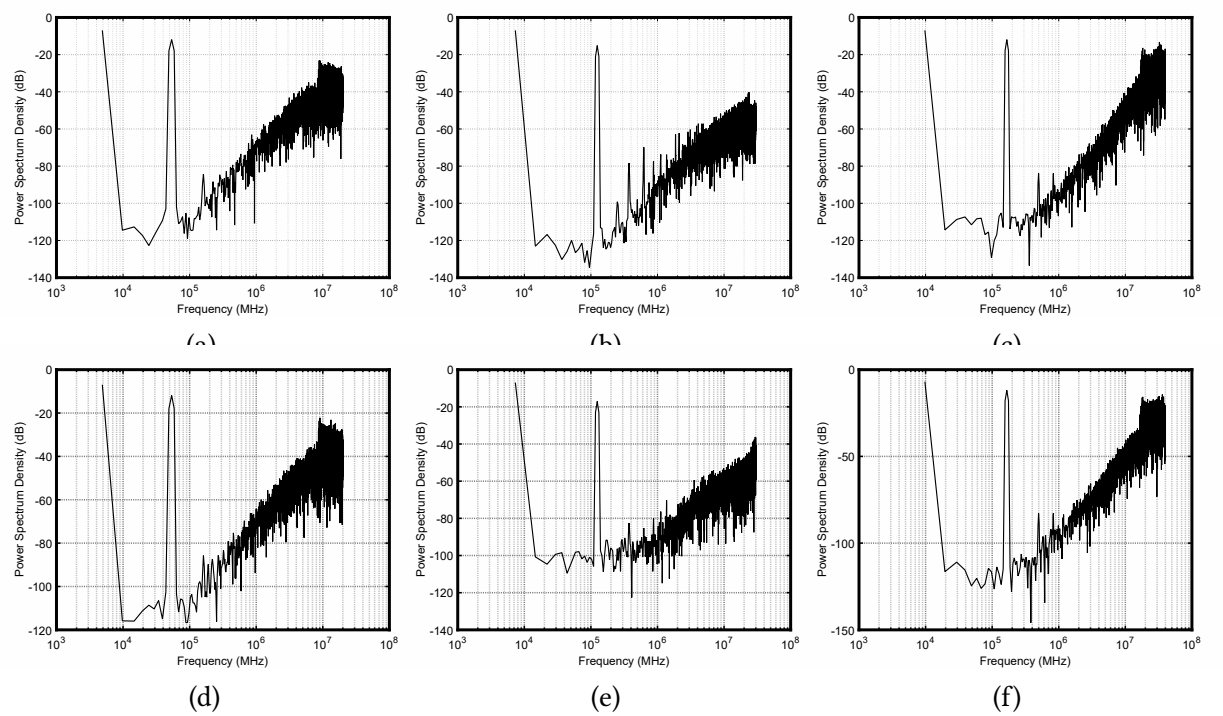


Figure 4.39: Power Spectrum Density for each mode of operation (Hanning Window with 8192 FFT points). Transistor-level simulation with ideal clock and OTA with 1.2 V transistors for (a) 40, (b) 60 and (c) 80 MHz; Transistor-level simulation with PLL-generated clock and OTA with 1.2 V transistors for (d) 40, (e) 60 and (f) 80 MHz.

For the integration using OTAs with 1.8 V transistors, the requirements were not met for any of the cases. The ENOB for GSM, BT and UMTS were respectively 10.55, 9.43 and 8.1 using ideal clocks. A severe degradation compared to the macro-model implementation and the integration using the OTAs with 1.2 V transistors. When PLL clocks are used there is also a degradation, resulting in 10.44, 9.43 and 7.94 respectively. The major contribution for this degradation is the limited output swing of the new OTAs, which causes distortion in the signal chain. Also, the limited SR also affects the modulators optimal performance.

Table 4.8 summarizes all results obtained and compares macro-model implementation with ideal clocks, macro-model with PLL-generated clock, transistor-level implementation with ideal clock and transistor-level implementation with PLL generated clocks. A comparison with other similar works is presented in table 4.9. The Figure-of-Merit (FoM) used is the Schreier FoM (PAVAN; SCHREIER; TEMES, 2017). It is the most widely used FoM

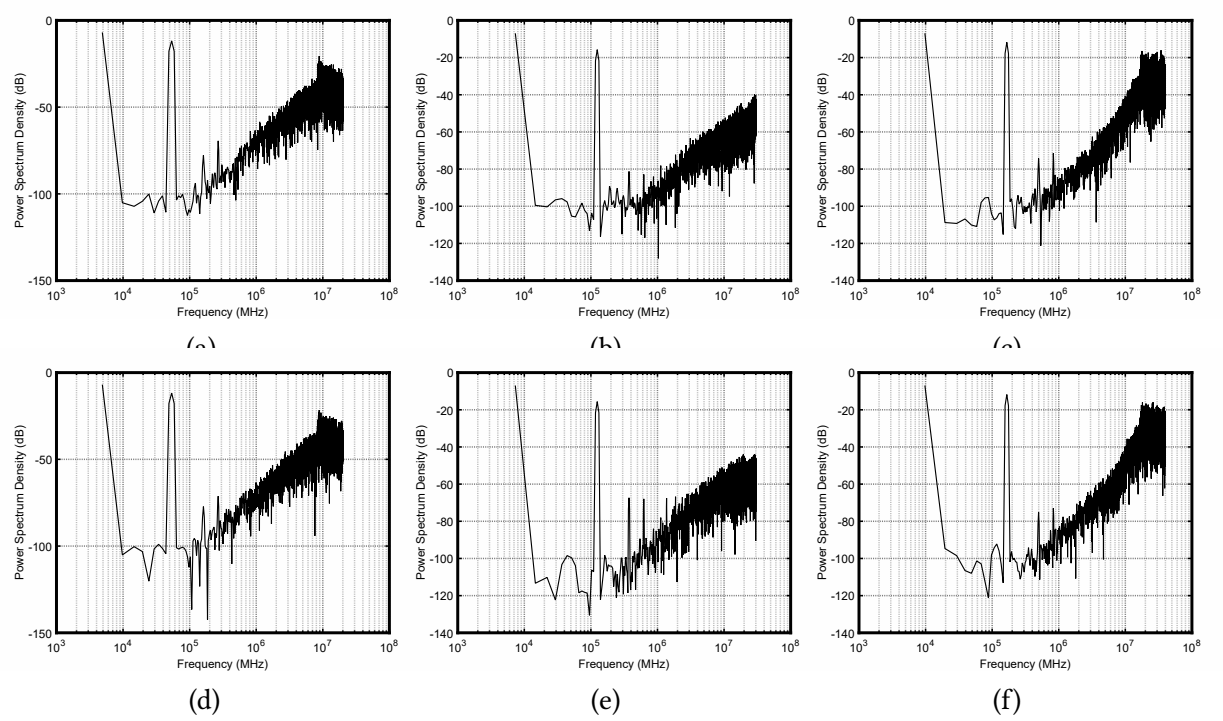


Figure 4.40: Power Spectrum Density for each mode of operation (Hanning Window with 8192 FFT points). Transistor-level simulation with ideal clock and OTA with 1.8 V transistors for (a) 40, (b) 60 and (c) 80 MHz; Transistor-level simulation with PLL-generated clock and OTA with 1.8 V transistors for (d) 40, (e) 60 and (f) 80 MHz.

for Data Converters, and relates the DR, Bandwidth and Power Consumption and is given by (4.5)

$$FoM_S(dB) = DR(dB) + 10log_{10}\left(\frac{BW}{P}\right) \tag{4.5}$$

Compared to other works a worst Figure-of-Merit result is obtained . (KE et al., 2010) and (CROMBEZ et al., 2010) employ CTΣΔM, which tend to be more power efficient due to the less demanding integrator settling. In (MORGADO; DEL RÍO, et al., 2010) extra care is taken in a dynamic bias scheme for the OTAs during lower frequency operation which helps improving the FoM for GSM and BT cases. (BETTINI et al., 2015) dynamically reconfigures the loop capacitors, altering the coefficients of the transfer function, thus improving performance. On top of that, all other works employ more complex loops (e.g. higher order loops and feedforward paths) and techniques (e.g. dynamic element matching in the feedback DAC), that should be utilized, in conjunction with the aforementioned techniques, in future iterations of this work to improve performance. Regarding the effects of poor clock performance, (CROMBEZ et al., 2010) highlights the effect of clock jitter, specially in the feedback DAC, in the modulators performance, however, none of the cited works effectively

Table 4.8: Comparison between Verilog-A models and transistor implementation for ideal *clock* and PLL generated *clock* (Worst case) applied to the modulator.

Parameter/Mode	**GSM**	**Bluetooth**	**UMTS**
Samp. Freq. (MHz)	40	60	80
Bandwidth (MHz)	0.2	0.5	2
Modulator Order	2^{nd}	2^{nd} 2.5 bit	3^{rd} 2.5 bit
Resolution Requirement (bits)	12	11	8
SNR Requirement (dB)	74	68	50

Verilog-A Models						
***Clock* Type**	**Ideal**	**PLL**	**Ideal**	**PLL**	**Ideal**	**PLL**
SNR (dB)	75	73	75.87	70.5	55.6	54.55
ENOB (bits)	12.15	11.88	12.31	11.44	8.94	8.77
SFDR (dB)	80	76.6	82.8	72.3	61.63	64.9
Transistor Implementation (1.2 V MOSFETs in the OTAs)						
***Clock* Type**	**Ideal**	**PLL**	**Ideal**	**PLL**	**Ideal**	**PLL**
SNR (dB)	71.1	71.73	63	61.2	54.87	53.71
ENOB (bits)	11.51	11.56	10.16	9.87	8.82	8.63
SFDR (dB)	72.35	73.84	63.23	65.5	65.62	63.21
Transistor Implementation (1.8 V MOSFETs in the OTAs)						
***Clock* Type**	**Ideal**	**PLL**	**Ideal**	**PLL**	**Ideal**	**PLL**
SNR (dB)	65.26	64.6	58.54	51.5	50.41	49.55
ENOB (bits)	10.55	10.44	9.43	8.26	8.1	7.94
SFDR (dB)	66	65.46	64.32	51.76	59.61	58.8

show a comparison of the obtained performance of the modulators for different jitter scenarios.

Additionally, to highlight the importance of macro-model simulation for debugging, the total simulation time for GSM, BT and UMTS were respectively 16, 28 and 32 minutes using macro-models, while for transistor-level the simulation (excluding the PLL generated clock) time for GSM, BT and UMTS took 36, 40, 44 hours respectively.

Table 4.9: Comparison with other works.

Reference	CMOS	Type	Supply (V)	Mode	BW (MHz)	SNR (bit)	P (mW)	FoM (dB)
This Work[1]	65 nm	DT	1.8	GSM	0.2	11.51	10.8	145
				BT	0.5	10.16	10.8	140
				UMTS	2	8.82	14.5	145
This Work[2]	65 nm	DT	1.8	GSM	0.2	10.55	7	140
				BT	0.5	9.43	7	130
				UMTS	2	8.1	10	142
(BETTINI et al., 2015)	130 nm	DT	1.2	EDGE	0.1	14.3	3.4	162
				UMTS	1.92	12.7	6.8	163
				LTE	5	12.4	18.8	161
					10	12	22.4	160
				LTE-A	20	10.9	44	154
					25	10.1	56.7	149
(KE et al., 2010)	90 nm	CT	1	GSM	0.2	13.8	2.8	164
				BT	0.5	12.7	2.6	161
				UMTS	2	12.1	3.6	162
				DVB-H	4	11.7	4.9	161
				WLAN	20	9.3	8.5	152
(CROMBEZ et al., 2010)	90 nm	CT	1.2	BT	0.5	13.6	5	163
				UMTS	1.92	12.6	6.4	162
				DVB	4	11.6	5.5	160
				WLAN	10	10.8	6.8	159
(MORGADO; DEL RÍO, et al., 2010)	90 nm	DT	1.2	GSM	0.1	12.1	4.6	148
				BT	0.5	11.1	5.3	148
				GPS	1	10.6	6.2	148
				UMTS	2	10.2	8	147
				DVB-H	4	9.5	8	146
				WiMAX	10	7.8	11	138

[1] OTAs with 1.2 V transistors
[2] OTAs with 1.8 V transistors
* Results from this work are obtained from transistor-level simulations. Other works results are from chip measurements.

Chapter 5

Conclusions

This work presented the complete development of a reconfigurable ΣΔ modulator to be used in multistandard wireless receivers that operate in GSM (BW = 200 kHz), Bluetooth (BW = 500 kHz) and UMTS (BW = 2 MHz), achieving an ENOB of 11.51, 10.16 and 8.82 bits, with a power consumption of 10.8, 10.8 and 14.5 mW and achieving a Schreier Figure of Merit of 145, 140 and 145 respectively.

To achieve the aforementioned reconfigurability and results, the proposed modulator operates as a second order modulator for GSM operation with a single bit quantizer and an oversampling frequency of 40 MHz. For BT operation, the modulator retains its second order noise-shapping, but replaces the single bit quantizer with a 5-level quantizer, and the oversampling frequency is increased to 60 MHz. Finally, for UMTS operation, the modulator operates as a 2-1 cascaded topology to achieve third order noise-shapping, with the 5-level quantizer and an increase to the oversampling frequency to 80 MHz. The frequency synthesis is realized with the implementation of a PLL circuit, operating from a single 10 MHz reference.

The development was based on the top-down/bottom-up methodology, following macro-model implementation, transistor-level implementation, and partial layout implementation. All sub-circuits were detailed both in macro-model and transistor-level implementation. The sub-circuits include: 1) OTA, 2) Comparators, 3) 5-level quantizer, 4) Switches, 6) Clock Synthesizer, 7) PFD, 8) CP, 9) LF, 10) VCO, 11) N-integer Frequency Divider, 12) Bias currents generators. Layout for the Clock Synthesizer was completed, and for the ΣΔM did not move forward due to problems in the design.

The biggest difference of this work compared to other reconfigurable ΣΔ modulators is the inclusion of the PLL-based clock synthesizer, and the effects of non-ideal clocks driving the sampling phase of the ADC. This subject has been gaining attention due to the extremely severe jitter requirements of new communication techniques, during transmission, reception and data conversion (RAZAVI, 2021), which are nearing tens of femtoseconds, and are already a major challenge for mixed-signals (specifically PLL, ADC and DAC) designers.

In conclusion, although no innovation was made in the designs of both the ΣΔM and Clock Synthesizer, the integration of both systems is not common in the related literature. On top of that, a lot of insight was gained in regards to the development and integration of high complexity systems, with the development of every sub-circuit, the integration of every sub-circuit in a ΣΔM, the integration of every sub-circuit in a PLL-based Clock Synthesizer, and of course, in the integration between both the ΣΔM and the synthesizer.

5.1 Future Works

Further improvements could be made in this project and are be listed below:

- The OTAs using the correct 1.8 V transistors are severely impacting the modulators performance. A topological change must be designed to increase the output voltage swing, which seems to be the major factor in the modulators degradation. Depending on the choice of topology, the use of 1.2 V for the supply voltage is also a possibility to allow more options of transistors in this PDK.
- The output digital filter and decimator must be implemented for a complete ΣΔ ADC.
- Robust voltage reference generators for the feedback DACs were not implemented. Simulations were performed using ideal DC sources.
- Improvements on jitter performance of the clock synthesizer must be implemented to reduce the modulators dedgradation.
- Integration with an external crystal oscillator is also still missing.

Future works related to this project are listed below:

- To achieve the higher frequencies of more recent standards related to 4G and 5G technologies, a reconfigurable SAR, Pipeline or hybrid topology are the best choices to further develop the reconfigurable ADC.

- With the inclusion of the modulator described in this work, combined with the ADC described in the previous item, a complete fully-reconfigurable ADC that operates in every current standard, ranging from 2G up to 5G, maintaining a reasonable power consumption for each standard is a feasible project, with no other comparable work reported.

- To achieve the frequencies of 4G and specially 5G standards the clock synthesizer design must be improved in regards to jitter performance. As described in (RAZAVI, 2021) jitter must be below 10 femtoseconds for the frequencies required in 5G operation.

5.2 Published Works

- (CASTRO et al., 2021a) M. Castro, R. Souza, Agord Júnior, L. Manera and E. Lima, "Modeling of Reconfigurable ΣΔ Modulator for Multi-standard Wireless Receivers in Verilog-A," 2021 34th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI), 2021, pp. 1-6, doi: 10.1109/SBCCI53441.2021.9529972.

Abstract: This paper presents the modeling and design of a reconfigurable ΣΔ modulator in Verilog-A language for applications in multi-standard wireless receivers. Main building blocks are implemented separately and its development detailed. Results presented are from simulations in SPECTRE circuit simulator in Cadence Virtuoso Analog Design Environment using Verilog-A models of main sub-circuits. The modulator achieves SNR values of 78.7 dB for GSM (EDGE) operation (200 kHz bandwidth), 79.9 dB for Bluetooth operation (500 kHz bandwidth) and 55.3 dB for UMTS (W-CDMA) operation (2 MHz bandwidth).

- (CASTRO et al., 2021b) Castro, M.B., Souza, R.R.N., Junior, A.M.P. et al. Phase locked loop-based clock synthesizer for reconfigurable analog-to-digital converters. Analog Integr Circ Sig Process 109, 647–656 (2021). https://doi.org/10.1007/s10470-021-01925-9

Abstract: This paper presents the complete design of a phase locked loop-based clock synthesizer for reconfigurable analog-to-digital converters. The synthesizer was

implemented in TSMC 65 nm CMOS process technology and the presented results were obtained from extracted layout view with parasitics. The synthesizer generates clock frequencies ranging from 40 MHz to 230 MHz considering a reference frequency of 10 MHz and a supply voltage of 1.2 V. Worst case current consumption is 634 μW, settling time is 6 μs, maximum jitter is 1.3 ns in a 0.037 mm^2 area. Performance was validated in a test $\Sigma\Delta$ Modulator with bandwidths of 200 kHz, 500 kHz and 2 MHz, and oversampling frequencies of 40, 60 and 80 MHz respectively, with negligible signal-to-noise ratio degradation compared to an ideal clock.

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