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Ultra-low Power Integrated Analog Front-End for ISFET-based Sensors

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Abstract—In this paper, an integrated analog front-end (AFE) to condition ISFET-based sensors is presented. This is accomplished by a pH-controlled ring oscillator (pHCO) that produces a pulse frequency-modulated signal proportional to pH of a testing solution. The AFE was designed in a 180-nm standard CMOS process and a Verilog-based model was used to aid electrochemical simulations. Sensorless measurements of the chip were carried out on the oscilloscope and results revealed a digitally-represented signal with 70 MHz/V of responsivity, under a sweeping voltage from 1.0 V to 1.2 V, and a worst-case scenario of 69.4 μ W for the overall power consumption. Moreover, the circuit topology circumvents the body effect problems, suppress the use of OP-AMPs or ADCs, and allows monolithic integration.

Index Terms—Chemical Sensors; ISFET; Analog Front-end; Conditioning Circuit; pHCO

I. INTRODUCTION

Over the past decades, and inspired by lifestyle and people's healthcare, the so-called wireless body area networks (WBANs) have engaged the attention of academical research referring to the control and monitoring of vital signals via highly integrated wireless sensing.

In a typical WBAN scenario (Figure 1), wireless sensor nodes installed in or on the human body are part of an instrumentation system designed to collect, monitor and transmit biomedical information of the patient such as body temperature, glucose level or infectious agents accountable for a variety of diseases. For this reason, circuits shall be designed to shrink their overall power consumption while still keeping a proper application performance [1].

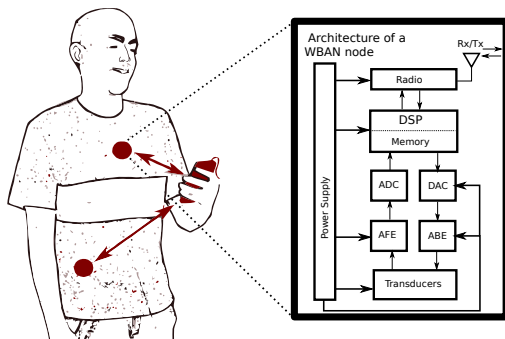


Fig. 1: WBAN node detail.

In a measurement system, sensors are used to convert a physical input variable on a corresponding electrical output.

As the electrical signal on its output is usually weak, an analog front-end (AFE) is required to condition the signal before conveying it to post-processing blocks. Therefore, the AFE plays an important role in the instrumentation system as it shall be designed to detect weak signals while ensuring information integrity to be subsequently shown.

Ultimately, the AFE design is further strongly dependent on the sensor features. One key advantage to select a suitable sensor element relies on assuring its compatibility with semiconductor fabrication methods, giving scope for monolithic integration of the sensors and intending to support the design of low-power, small-sized and fast response time systems. Between this and that, we present in this work an integrated AFE design for an ISFET-based sensor that can be used for glucose measurement in a WBAN sensor node.

The ISFET, Ion-sensitive Field-effect Transistor, is a chemically sensitive FET conceived in 1970 by Bergveld [2] and, thenceforth, it has been used as a biosensor due to its potentiality to be functionalized and to sense pH levels arising from redox reactions. Its insulating membrane is sensitive to hydrogen ions in the test solution, in such way any change in the pH level charges a potential profile across the solution causing, thus, a modulation in the ISFET threshold voltage. A comprehensive review of ISFET functionalization and other FET-based biologically sensitive FETs can be found in [3].

Despite the progress on the design of input stages, much of the previous works has primarily focused on two AFE topologies for ISFET: the source-drain followers [4] and the differential pair schemes [5]. The first one demerits the ISFET's transistor-like behaviour by forcing a single operating point on it at constant drain-to-source voltage and constant drain current to track changes in the threshold voltage caused by a pH level fluctuation. In addition, this configuration suffers from body bias effect, which undertakes the readout sensitivity of the circuit. On the other hand, the differential pair provides benefits by virtue of its common-mode rejection, although its realization in practice is challenging due to differences between the ISFET threshold voltage and its MOSFET counterpart. Both configurations output a voltage proportional to the pH of testing solution. A final and equally important point is that AFE circuits are generally used to hold the information upon the electrical signal amplitude, therefore, requiring an analog-to-digital converter (ADC) which accounts for further circuit design, silicon area and power consumption.

In this work, we report the design of an AFE that converts the pH information automatically to digital domain via pulse-frequency modulation (PFM), therefore, overcoming the ADCs use in the system. This was solved by a pH-controlled ring oscillator (pHCO) whose current is controlled by the pH level arisen upon the sensor surface, so that the output signal becomes digitally-represented by the pH level.

II. SHORT REVIEW OF ISFET OPERATION

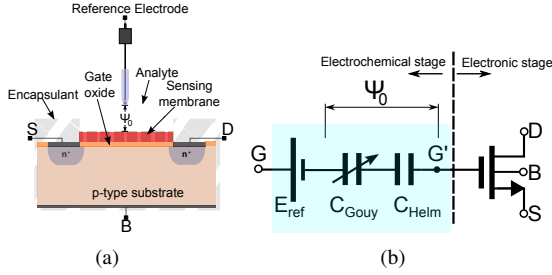


Fig. 2: (a) ISFET device; (b) Behavioral ISFET model

ISFETs are ion-sensitive electrochemical sensors being derived from a simple MOSFET (Figure 2(a)), in which its gate terminal is coated with a material used to sense ions concentration (usually H^+).

The principle of ISFET operation is related to chemical reactions happening in the oxide-electrolyte interface. Such mechanisms are best described by the site-binding and electrical double layer theory [6], where H^+ ions presented in the analyte are adsorbed by the sites presented in the hydrated oxide surface producing a potential profile (Ψ_0) across Gouy-Chapman and Helmholtz capacitances (Figure 2(b)). The potential profile is proportional to the pH as stated in the general expression of the ISFET pH sensitivity:

$$\frac{\partial \Psi_0}{\partial pH} = -2.3 \cdot U_T \cdot \alpha, \quad (1)$$

where $U_T = kT/q$ is the thermal voltage and α a dimensionless parameter ranging between 0 and 1 that relates the degradation of ISFET responsivity to the ideal Nernstian responsivity (59 mV/pH).

III. ISFET FABRICATION

The ISFET devices used were designed and fabricated at the Centro de Componentes Semicondutores (CCS), Unicamp, Brazil. The first batch furnished was organized in an array comprising 3x19 sensing elements with 50 μm /50 μm of aspect ratio each using a TiO_2 (Titanium dioxide) film (refer to Figure 3).

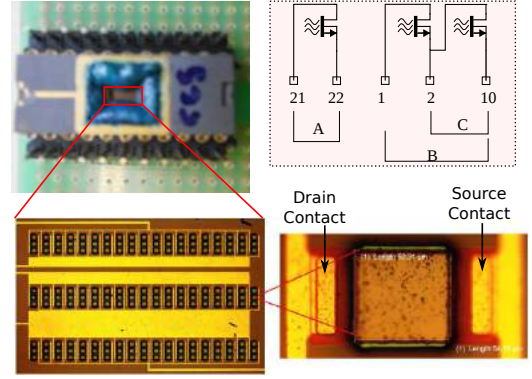


Fig. 3: Top left: photo of the encapsulated ISFET chip fabricated. Lower left: ISFETs matrix (3x19) from the view of an optical microscope. Bottom right: Detail of the sensor array elements. Top right: Welding diagram of the chip

A short description about the main process steps of the ISFET's fabrication is presented in the cross sections of Figure 4.

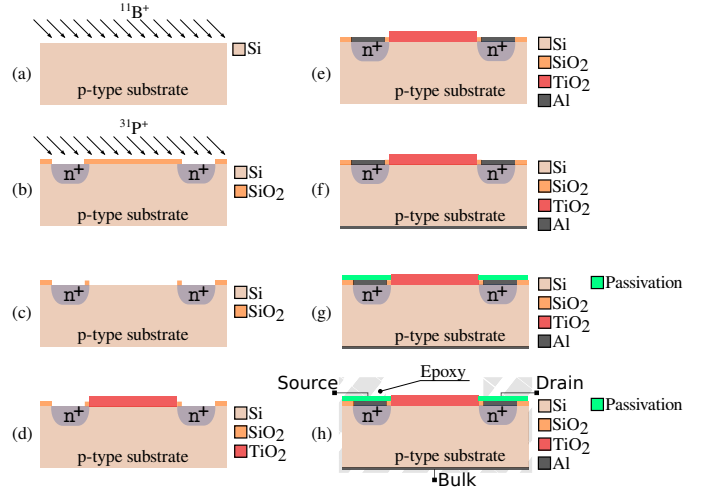


Fig. 4: Process steps for ISFET's fabrication.

The start material was a p-type single-crystal silicon wafer with a crystallographic orientation of $< 100 >$ and resistivity ranging from 1 to 10 $\Omega \cdot cm$.

Initially, a 4×10^{13} ions/ cm^2 boron implantation dose was used to adjust the threshold voltage evenly over the entire wafer (Figure 4(a)). Then, a wet oxidation step took place at 1000 $^\circ C$ to grow 1- μm of field silicon dioxide.

The first mask of the photolithographic step was used to define the source and drain regions. After development of the photoresist, a phosphorous dose of 7×10^{15} ions/ cm^2 was implanted in the diffusion regions and followed by an annealing step at 1000 $^\circ C$, for 30 minutes, in N_2 environment, for dopant activation (Figure 4(b)).

Next in order, the second mask defined the contact openings for the diffusion regions and the gate area where the sensitive film (TiO_2) was deposited (Figure 4(c)). The film was obtained by rapid thermal oxidation and annealing for 40 seconds at 960 $^\circ C$ after sputtering 10-nm of Ti on the wafer (Figure 4(d)). One should notice here that the Ti deposited on

non-gate areas were removed by lift-off process, with acetone, before the thermal oxidation step. In addition, since the TiO_2 is a well-known biocompatible material, its use as a sensitive film supports a large range of biomedical applications for the ISFET.

The third mask defined the contact openings for source and drain regions. Aluminum (Al) with 1% of Si was sputtered to deposit 300-nm of contact film (Figure 4(e)). Then, the native SiO_2 on the backside of the wafer was wet etched with BHF (Buffered Hydrofluoric Acid) and the same Al thickness sputtered to create the body contact (Figure 4(f)). The wafer was then annealed in a conventional furnace filled with forming gas at 430 °C, for 10 minutes, to reduce the contact resistance.

Finally, the contacts were passivated with the photoresist AZ 4620 so the samples can be used in a wet environment alongside the analyte. Only the gate sensing areas remained exposed (Figure 4(g)). The wafer was later diced, wire-bonded with gold and packaged. The wire bindings were insulated using epoxy resin (Figure 4(h)).

After all, the samples were characterized and the electrical parameters used to feed a Verilog-A behavioral model in order to aiding the CAD simulations.

1) *Sensor Characterization*: The parameter extraction used in the testing devices was based on the g_m/I_D methodology [7]–[9]. The setup measurement is shown in Figure 5.

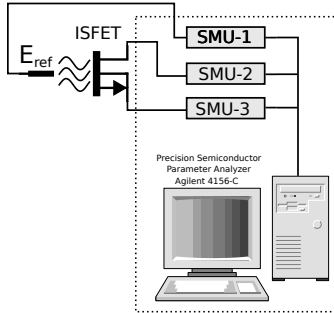


Fig. 5: Setup measurement used for the sensor characterization.

In this setup, the gate voltage V_G was swept from 0 V to 2.0 V on the SMU-1 (Source-Measurement Unit) under a fixed drain voltage V_D forced at half of the thermal voltage, i.e. 13 mV, on the SMU-2. The circuit's reference voltage (ground) was forced on the SMU-3.

Next in order, the g_m/I_D device characteristic curve was generated and used to find the equilibrium threshold voltage (V_{TO}) and the specific current of the model (I_S). The curve in Figure 6 depicts the point at which g_m/I_D drops to 53 % of its peak value [9]. The gate voltage measured at this point corresponds to V_{TO} , and the corresponding drain current is approximately the specific current I_S . From this current, K_P parameter was found, since:

$$K_P = \mu C'_{ox} = \frac{I_S}{\frac{W}{L} n \frac{\phi_t^2}{2}} \quad (2)$$

where ϕ_t , in Equation (2), refers to the thermal voltage.

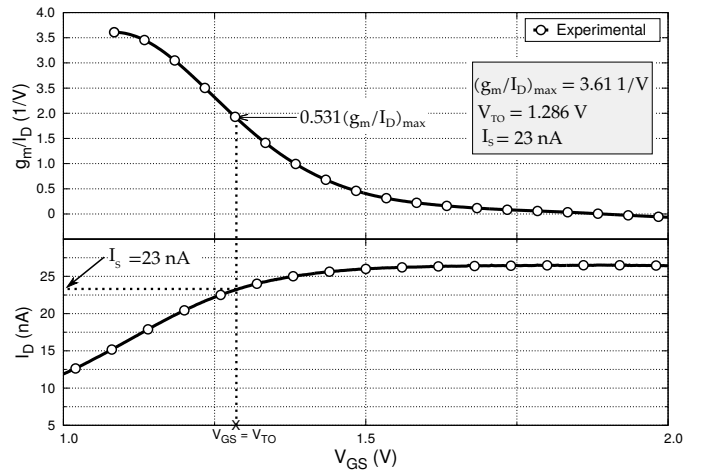


Fig. 6: Parameters obtained with the experimental results: equilibrium threshold voltage (V_{TO}), specific current (I_S) and the maximum transconductance-to-current ratio $(g_m/I_D)_{max}$.

The results found were then used in the Verilog-A electronic stage as reported in Table I.

Parameters	Value
V_{TO}	1.286 V
I_S	23 nA
$(g_m/I_D)_{max}$	3.61 1/V
K_P	1 $\mu A/V^2$
W/L	2850 μm / 50 μm

TABLE I: Sensor characterization results

One can notice that the $(g_m/I_D)_{max}$ is way below the expected values for MOSFET (25 - 30 V^{-1}) devices. However, differently from genuine MOSFETs, in the case of ISFETs, the charge density control in the channel has a capacitive divider at the input coming from the electrochemical stage (Gouy-Chapman and Helmholtz capacitances) that is accountable to degenerate its $(g_m/I_D)_{max}$.

With both chemical and electronic stages duly supplied, we have plotted the IxV simulation characteristic curve and fitted it with the experimental results found. That being necessary because of shifts arisen from imbalances over the fabrication process. In our experiment, higher contact impedances at source-and-drain diffusion regions were found, as reproduced in Figure 7 by the slightly S-shaped curve around the very beginning of linear region over the experimental results.

IV. REVIEW OF MAIN ISFET INTERFACE CIRCUITS

This section overviews the main topologies employed for ISFET conditioning.

A. Source-drain followers

One of well-known topologies are those whose the ISFET electrical signal is sensed from source-drain follower schemes [4]. The main idea behind these structures is to bias the ISFET with constant drain-to-source voltage and drain current (CVCC), while maintaining reference electrode at a constant

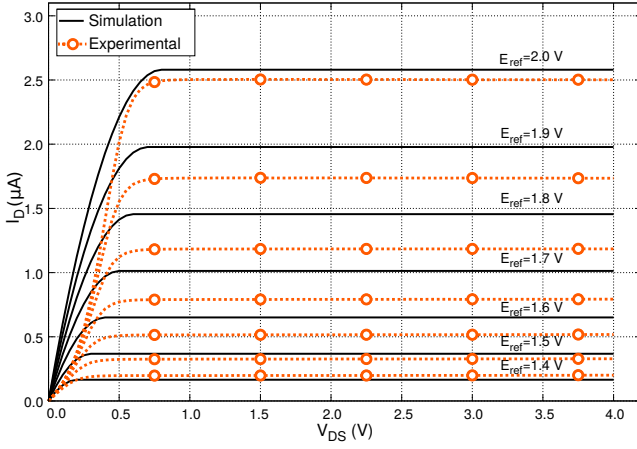


Fig. 7: Fitting between simulation and experimental curves of the ISFET-based sensor testing device.

potential (usually ground) - Figure 8. However, due to the presence of a non-zero V_{SB} voltage in this topology, second-order temperature effects are introduced and a parasitic change in V_{TH} is observed, affecting, thus, the conditioning circuit performance.

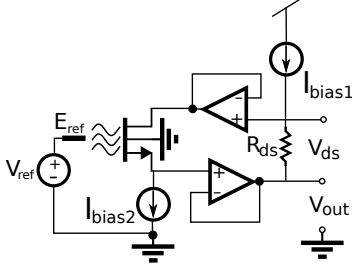


Fig. 8: Source-drain follower topology.

B. ISFET/MOSFET Currents Equalization

To overcome the body effect drawbacks, the work presented in [10] reports an interface circuit to equalize the ISFET current and the current of constant current source by means of direct feedback to reference electrode (Figure 9(a)) or indirect feedback to current source, Figure 9(b). In the direct feedback structure, the output is sensed in the reference electrode. The scheme is simple, but it may suffer from stability issues due to the two high impedance nodes in the feedback structures - as already pointed in [11].

C. Differential pair

Some others approaches employ differential schemes such as ISFET/MOSFET, ISFET/REFET and ISFET/ISFET differential topologies to perform temperature compensation via common-mode rejection. The ISFET/MOSFET pair is difficult to implement due to the explicit intrinsic differences in threshold voltage pair, resulting in a bias difference and mismatch [2]. By this reason, ISFET/REFET pair is more used since when connected in a differential mode produces a strictly pH sensitive output. Unfortunately, a stable attachment usually

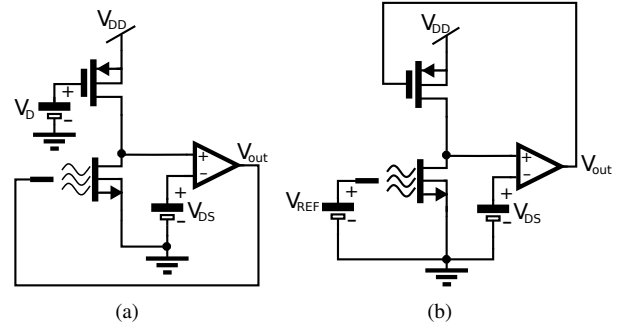


Fig. 9: Complementary ISFET/MOSFET pair topologies: (a) direct feedback; (b) indirect feedback

comes with a polymer with a given resistivity accountable for changing the electrical relaxation time, which is a measure for the time needed to redistribute the charge and establish potential profiles in the polymer after application of an electrical field [2].

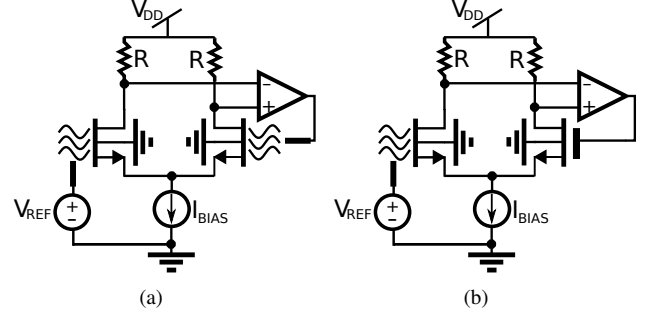


Fig. 10: Differential pair topologies: (a) ISFET-ISFET; (b) ISFET-MOSFET

D. Time domain approaches

Exploring both time and digital domains, authors in [12] have proposed a readout scheme with minimum analog components to minimize parasitic and noise effects in large-scale chemical sensing arrays (Figure 11). For each array pixel, a pair of complementary ISFETs shares the same floating gate in an inverter configuration whose output is a chemically-controlled pulse-width modulated signal. In [13], an ISFET averaging array employing global negative current feedback is used to modulate VCO frequency of a first order sigma-delta modulator.

V. DESCRIPTION OF THE PHCO PROPOSED

The AFE topology presented in this work, and henceforth named as pHCO, obtains the pH information using a pulse-frequency modulation technique, as shown in Figure 12.

In this scheme, the sensor's electrically-weak signal becomes digitally-represented by virtue of the AFE so that the pulse frequency is proportional to the pH level of a testing solution. Therefore, we have eliminated the power-consuming ADC from the instrumentation system, thus, solving for system complexity, power constraints and further block design.

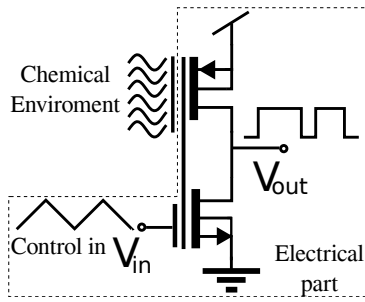


Fig. 11: PWM-based readout scheme for ISFET-based sensor.

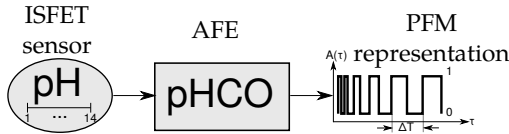


Fig. 12: Conceptual design of the ISFET conditioning system using PFM.

In addition, signal-amplitude saturation issues affecting some topologies - because of the OP-AMPs usage in feedback mode - are no more a prominent drawback. Moreover, one may note that this topology eliminates the body effect problems, due to constant $V_{SB} = 0$ bias of ISFET.

A. Dynamic analysis of the pHCO

The pHCO circuit comprises an N-stage single-ended ring oscillator in which the delay stage has a CMOS inverter on a push-pull configuration. The number N of stages to be considered shall affect the expected oscillation frequency as per Equation (3), [14]:

$$f_o = \frac{1}{N \cdot T_p}, \quad (3)$$

where T_p is the propagation time of the inverter cell.

All nMOS sources included in the ring oscillator are connected to the drain contact of the diode-connected ISFET. Therefore, the ISFET operation can be described as the current source controlled by the potential V_{chem} as reproduced in Figure 13.

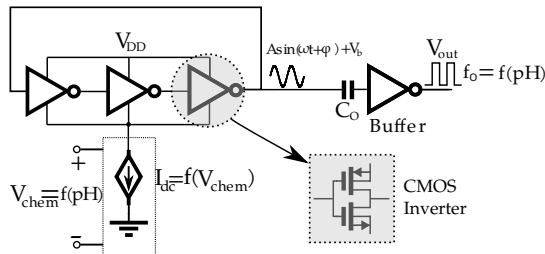


Fig. 13: Conceptual representation of the pHCO circuit

As long as inverters operate as linear amplifiers, the ring oscillator outputs a sinusoidal signal of amplitude A, frequency ω and DC level V_b - all pH-dependent. Since the DC level is removed by capacitor C_o and, afterwards, the buffer gain saturates the signal amplitude, output V_{out} produces digital

pulses whose pH information is encoded only in the frequency domain.

B. Static analysis of the pHCO

Figure 14 reproduces, in short, the self-biasing circuit used to establish the ISFET DC operating point. In this figure, the ring oscillator is represented by the active load Z_L , while V_{chem} denotes for a pH-dependent potential arising upon the ISFET surface.

As a pH change produces a V_{chem} change, a current of value I_D shall be established producing, when passing through Z_L , the potential V_G . This potential, when compared to the setpoint V_{chem} , produces the error voltage V'_G - accountable to establish the operating point of I_D , as a result. This self-biasing circuit is realized via serie-series feedback, as depicted by Figure 14.

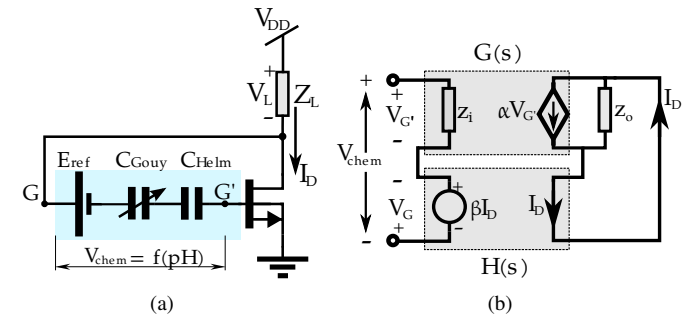


Fig. 14: Static analysis of the pHCO: (a) Simplified circuit representation. (b) Diagram addressing local negative feedback.

C. Integrated Circuit Design

The IC was designed in a 180-nm standard CMOS process and the design flow realized over the IC design is represented in Figure 15.

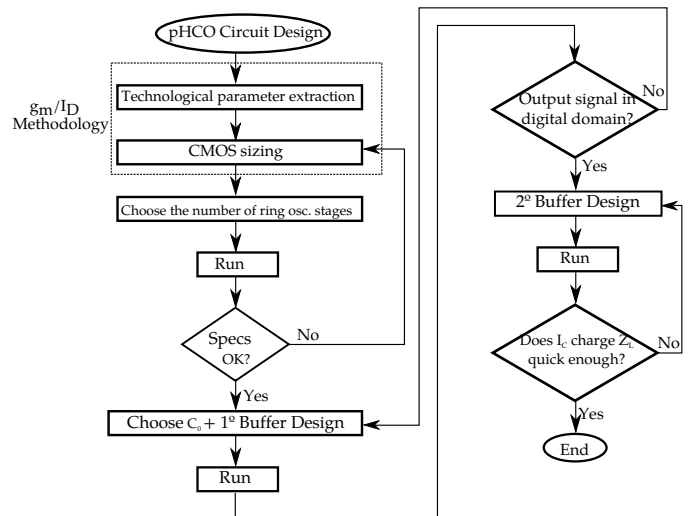


Fig. 15: Flowchart describing the circuit design assumed

Firstly, nfet and pfet devices - included in the PDK - were characterized via g_m/I_D methodology. The g_m/I_D curve

was plotted and used to define MOSFET sizing included in the CMOS pair [15]. Secondly, a number of stages for the ring oscillator was defined. Once the power consumption, the linearity and the robustness specifications were met, the next step consisted on the calculation and the sizing of the decoupling capacitor C_0 . Next, a buffer was designed to assure digitally-represented signal output. Lastly, another buffer was designed to meet the signal measurement requirements on the oscilloscope.

1) *The g_m/I_D methodology*: The transconductance-to-current-ratio method has the advantage of being based on a physical property of the device, and thus being independent of a specific model [9]. Additionally, the g_m/I_D is a figure of merit which describes the efficiency of current conversion in transconductance. Furthermore, the choice of this method was based in two main reasons:

- It provides an indication of the transistors' DC operating point; and,
- It allows a proper transistor sizing.

The parameter extraction was performed using same procedure reported over the sensor characterization. After plotting g_m/I_D and $I_D \times V_G$ transfer curves, the following parameters were found:

180-nm PDK		
	I_{SQ} (nA)	V_{TO} (mV)
nfet	134	362.5
pfet	27	-103

TABLE II: Device characterization of the 180-nm standard CMOS PDK

where I_{SQ} denotes for the specific current I_S found by squared-devices. Moreover, the relationship between g_m/I_D and the transistor operating point can be noticed since this ratio is the derivative of the I_D logarithm compared to V_G , as it follows [8], [9]:

$$\frac{g_m}{I_D} = \frac{1}{I_D} \frac{\partial I_D}{\partial V_G} = \frac{\partial \ln I_D}{\partial V_G}. \quad (4)$$

Since g_m/I_D versus inversion coefficient (i_f) curve was plotted, an operating point could be chosen for transistors sizing.

One can observe, from Figure 16, a 31 V^{-1} and 29 V^{-1} of uppermost g_m/I_D in the very deep weak-inversion mode for pfet and nfet devices, respectively. Nevertheless, a 0.1 of i_f (weak-to-moderate inversion mode) for both transistors was chosen as operating point intending to relax likely process variations.

As a result, aiming a current equal to 100 nA and based on Equation (5), one can obtain the following transistors sizes.

$$\left(\frac{W}{L}\right) = \frac{I_D}{I_{SQ} i_f}, \quad (5)$$

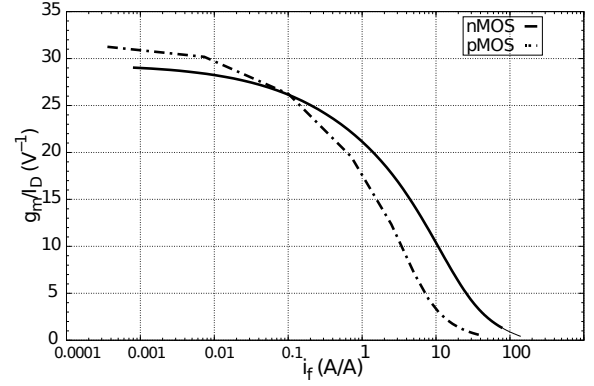


Fig. 16: Transfer curve obtained with a DC simulation of the nfet and pfet devices included in the IBM 0.18 μm technology

$$\left(\frac{W}{L}\right)_n = \frac{100 \text{ nA}}{134 \text{ nA} \times 0.1} \approx 8, \quad (6)$$

$$\left(\frac{W}{L}\right)_p = \frac{100 \text{ nA}}{27 \text{ nA} \times 0.1} \approx 37. \quad (7)$$

From the calculated aspect ratio, we have found, after simulation, the following transistor sizes for nfet and pfet devices.

Aspect Ratio	Value ($\mu\text{m}/\mu\text{m}$)
$(W/L)_n$	16/2
$(W/L)_p$	74/2

TABLE III: Aspect ratio calculated for the nfet and the pfet devices after simulation

Next, we have introduced the sensor to the AFE in order to verify the switching threshold point (V_{SW}) via DC sweep simulation. As the value observed for V_{SW} was above the half rail voltage, we have resized the pfet width from 74 μm to 50 μm . It is clear that resizing the aspect ratio changes the bias condition and hence g_m/I_D . However, this change holds a minor influence in the final operation of the circuit since the dynamic range and linearity at the output remained roughly unchanged. One can observe, from Figure 17, the CMOS transfer curve over pH 4, pH 7 and pH 10.

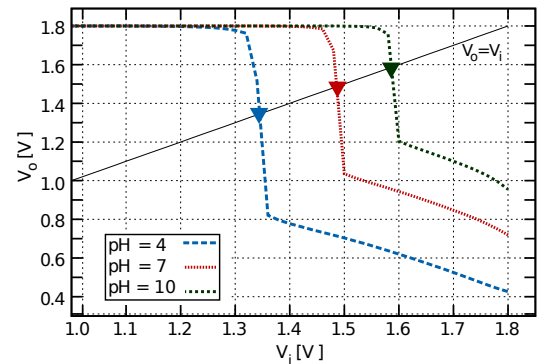


Fig. 17: CMOS transfer curve obtained via DC simulation, over pH 4, pH 7 and pH 10 and with the ISFET connected to nfets sources

2) *Number of CMOS stages*: The number of stages was decided based on the power dissipation minimization, silicon area and the responsivity aimed. As stated in Equation (9), the overall power consumption can be expressed by a combination of static (P_E), dynamic (P_D), and short-circuit (P_{CC}) power terms [16].

$$P_{TOTAL} = P_E + P_{CC} + P_D, \quad (8)$$

$$= N \left(V_{DD} I_L + V_{DD} \hat{I}_P \tau_{cc} f_0 + V_{DD}^2 f_0 C_L \right), \quad (9)$$

where V_{DD} stands for the power supply, I_L the current across the load, \hat{I}_P the peak current, τ_{cc} the short-circuit time duration, f_0 the oscillation frequency and C_L the load capacitance. One can notice the power consumed decreases proportionally to the number of stages - for a fixed value of V_{DD} and C_L . As a result, we have designed a single-ended ring oscillator with minimum number of stages: three.

3) *First Buffer and C_0 Design*: The first buffer design placed the switching threshold voltage at $V_{DD}/2$ and, additionally, provided the necessary gain to digitally represent the signal using minimum transistor dimensions.

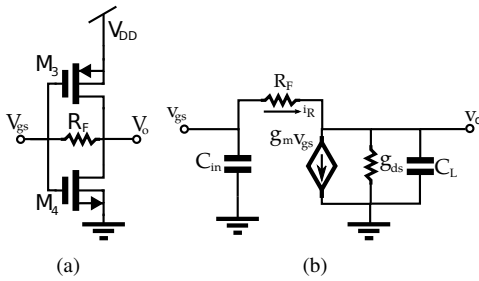


Fig. 18: Design of the first buffer

(a) Topology assumed (b) Small-signal model of the CMOS stage.

A single-ended CMOS inverter with a feedback resistor (R_F) connected between output and input was the topology used - as represented in Figure 18. The key role of R_F resistor relies on the equalization of DC common mode voltage between input and output; in other words, forcing $v_o = v_{gs}$. This was achieved by trading the circuit gain, as stated in Equation (10).

$$\frac{v_o(s)}{v_{gs}(s)} = \frac{-(g_m + R_F^{-1})}{g_{ds} - R_F^{-1} + sC_L}. \quad (10)$$

In addition, as stated by Miller's theorem, R_F reduces by $1 + A_0$ times the equivalent input resistance - where A_0 denotes for the stage gain. Therefore, the small-signal circuit resulted shall be represented as per Figure 19(b).

The virtually reduced resistance owing to the Miller effect, associated with the capacitance C_0 , adds a pole in a frequency ω_p about to:

$$\omega_p = \frac{1}{R'_F C_0}, \quad (11)$$

where $R'_F = R_F / (1 + A_0)$ is the effective value of resistance related to the input node owing to the "Miller" effect. After running a circuit simulation, a 510-k Ω R_F resistance

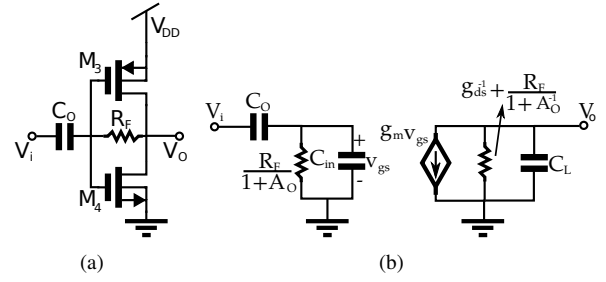


Fig. 19: First buffer design

(a) Gain stage with the C_0 capacitor connected to the input
(b) Small-signal equivalent model of the buffer using the "Miller" approximation.

was found, which let, afterwards, to find the value of the capacitance C_0 . For this, a cut-off frequency three times lower than the lowest frequency (1 MHz) was chosen (Equation 12) yielding about 12-pF capacitance.

$$C_0 = \frac{1}{2\pi R'_F f_c} \approx 12 \text{ pF}. \quad (12)$$

4) *Second Buffer Design*: A second buffer was designed to enable a proper signal measurement on the oscilloscope. To cope with this, a value of current was calculated to charge the impedance probe ($R = 10 \text{ M}\Omega$ and $C = 16 \text{ pF}$) to a 1.8 V of supply voltage in a time period lower than the signal having the lowest time period. Considering the following design specifications used:

- Signal's period with topmost frequency: $T = 30 \text{ ns}$
- Probe's capacitance: $C = 16 \text{ pF}$

the value of current that meets the aforementioned specifications shall be:

$$I_c = C \frac{\Delta V_c}{\Delta t} = 16 \text{ pF} \times \frac{1.8 \text{ V}}{20 \text{ ns}} = 1.45 \text{ mA}. \quad (13)$$

Consequently, the CMOS transistors were sized to convey a 1.45 mA of DC current to the load. Simulation results over pH 4, pH 7 and pH 10 (Figure 20) have denoted that the output signal can be measured by an oscilloscope probe.

The circuit schematic in transistor level with the values used in each circuit component is shown in Figure 21.

The layout sent to fabrication is shown in Figure 22. The red frame denotes the area where the pHCO circuit was fabricated. ESD protection circuits were placed on the PADs.

VI. POST-LAYOUT SIMULATION RESULTS

This section presents the post-layout simulation results considering two types of ISFET to be addressed:

- ISFET A, comprising an array of 3x78 elements; and,
- ISFET B, comprising an array of 3x57 elements.

A Verilog-based model was designed to aid over the electrochemical simulations and its electrical parameters found after an electrical characterization of an available ISFET sample.

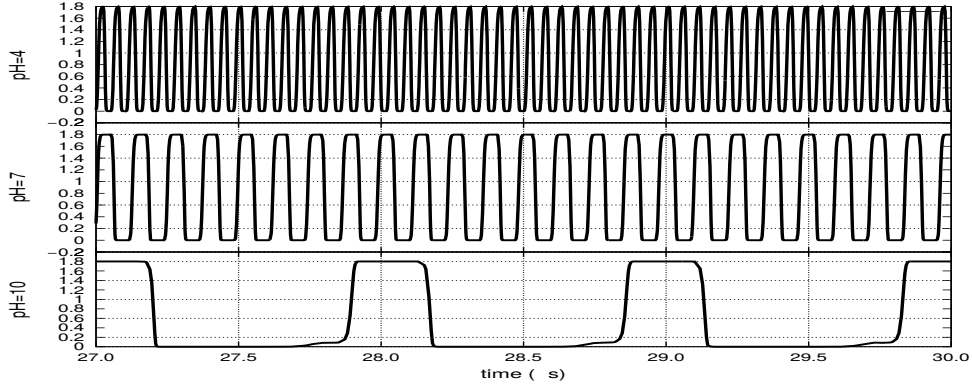


Fig. 20: Transient simulation of the output signal for pH 4, pH 7 and pH 10

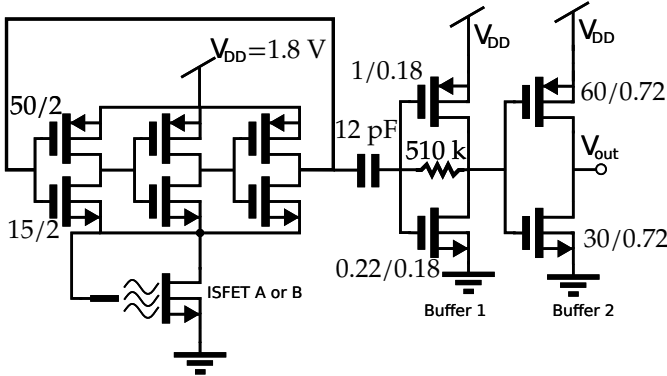


Fig. 21: Detailed schematic of the pHCO integrated-circuit with the values used in each component

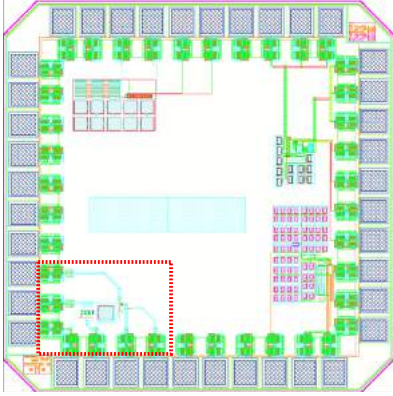


Fig. 22: The fabricated chip comprising the pHCO circuit layout inside the red frame.

A. Transfer curve

Figure 23 reproduces the transfer curve found between oscillation frequency and pH for ISFET A and B. Its graphical difference to the ideal linear model (trendline) is better depicted by the error curve whose Y-axis is represented on the right side of the graph. A R^2 coefficient of 0.9866 and 0.9903, and an uppermost non-linearity error of about 12 % were found for ISFET A and B, respectively, denoting, thus, a good fit with the linear model. Additionally, one can find, from these figures, the trendline terms obtained in each case.

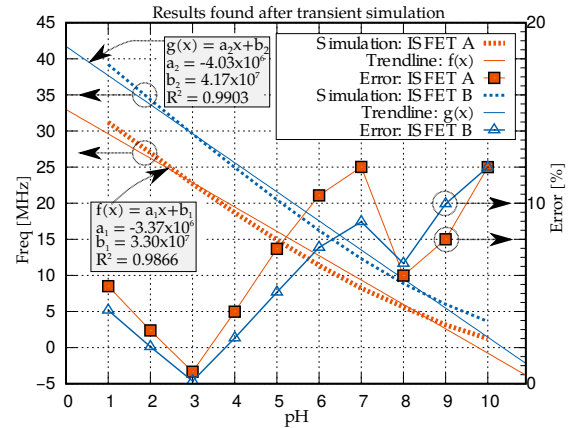


Fig. 23: Transfer curve observed between the output signal frequency and the pH (obtained via transient simulation).

1) *Monte Carlo*: A Monte Carlo simulation over 200 samples was ran for oscillation frequency and overall power consumption. Its results are found in Figure 24 and its probability distribution includes the mean, minimum, maximum and standard deviation found for the samples.

2) *Corners*: Corner simulation results, reproduced in Table IV, were performed in seven different corners bounded by the process. A 75.6 μW and 76.1 μW of minimum, and 171 μW and 174 μW of maximum overall power were found for ISFET A and B respectively. 8.75 MHz and 10.1 MHz of nominal oscillation frequency with 114 μW and 113.6 μW of nominal overall power were found for ISFET A and B, respectively.

VII. MEASUREMENT RESULTS OF THE FABRICATED CHIP

The circuit was measured using a sweeping voltage source to emulate the ISFET operation, as shown in Figure 25(a). Thus, sensorless measurements on the oscilloscope were carried out to ensure that the herein proposed AFE works properly and likewise draw its performance.

The oscilloscope measurements revealed that the output signal V_{out} remains digitally-represented over the range from 1.0 V to 1.3 V when sweeping V_{REF} voltage. The current and frequency for each sweeping point were measured and the overall power consumption estimated from the results (Table V).

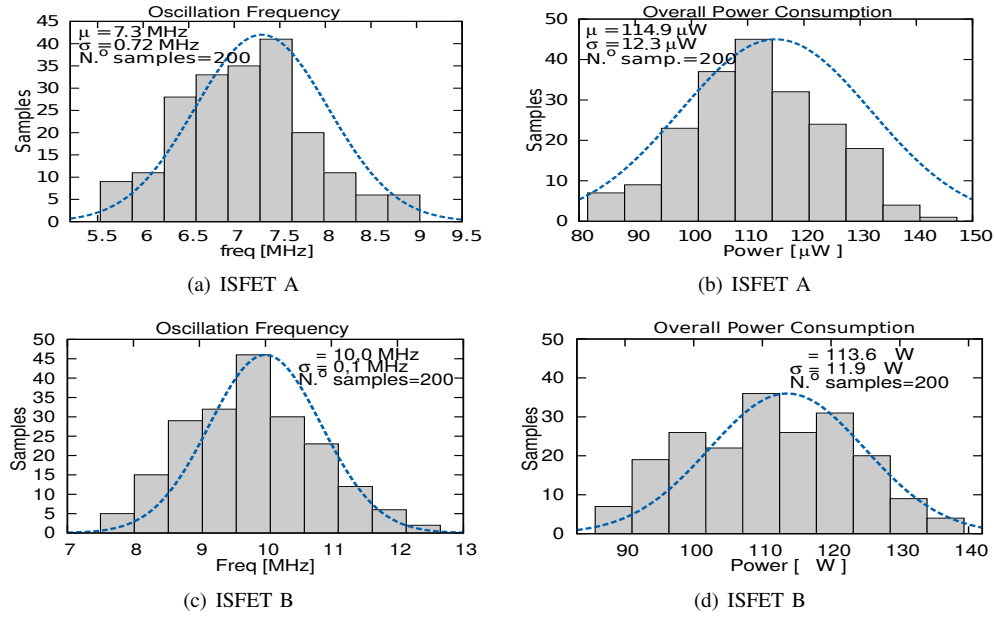


Fig. 24: Post-layout Monte Carlo result for 200 samples

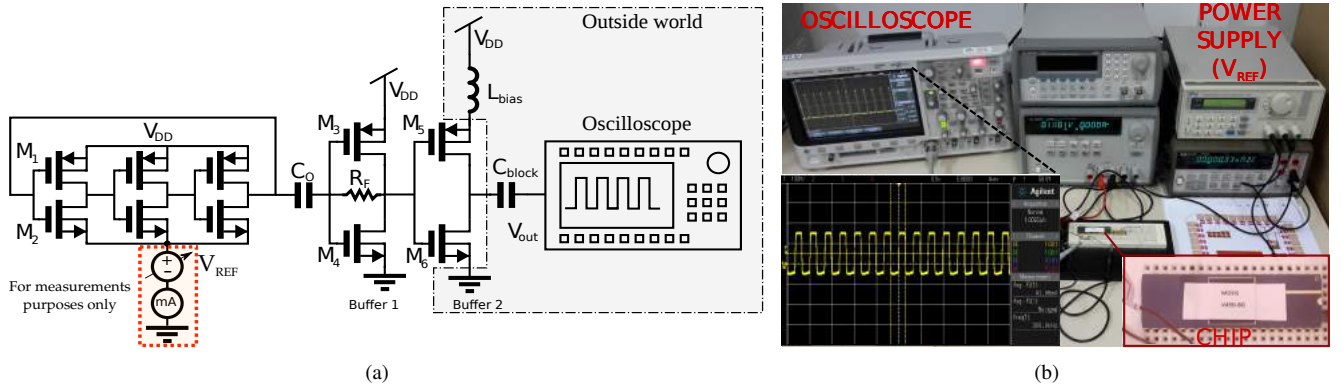


Fig. 25: (a) The pHCO integrated-circuit sensorless setup measurement (b)Photo of the chip setup measurement in the oscilloscope.

	ISFET A		ISFET B	
Corners	Frequency (MHz)	Power (μW)	Frequency (MHz)	Power (μW)
Nominal	8.75	114	10.1	113.6
ff	11.2	149	13.0	152
fff	12.5	171	14.6	174
ss	6.79	88.0	7.70	88.8
ssf	5.85	75.6	6.55	76.1
fs	9.90	118	11.3	120
sf	7.73	109	8.49	110
Min.	5.85	75.6	6.55	76.1
Max.	12.5	171	14.6	174

TABLE IV: Results for oscillation frequency and overall power in the corners

According to Table V, the estimated worst-case scenario for the overall power consumption was $69.4 \mu W$ - this being inferior to the simulation results because of the ISFET absence in the experiment.

V_{REF} (V)	I (μA)	f_o (MHz)	Power (μW)
1.0	38.6	17.4	69.4
1.1	18.3	10.4	32.9
1.2	4.5	3.5	8.1
1.3	0.1	0.46	0.18

TABLE V: Summary of the chip experimental results without ISFET

Some of the waveforms acquired on the oscilloscope, after V_{REF} voltage sweep, are depicted in Figure 26.

Digitally-represented waveforms for the output signal, as well as the PFM behaviour when sweeping V_{REF} , can be verified from Figure 26 evidencing, thus, the appropriate AFE role. Moreover, the circuit presents a R^2 coefficient of 0.9999, less than 0.5 % of linearity error and a responsivity of about 70 MHz/V - over the sweep from 1.0 V to 1.2 V - which address its good performance.

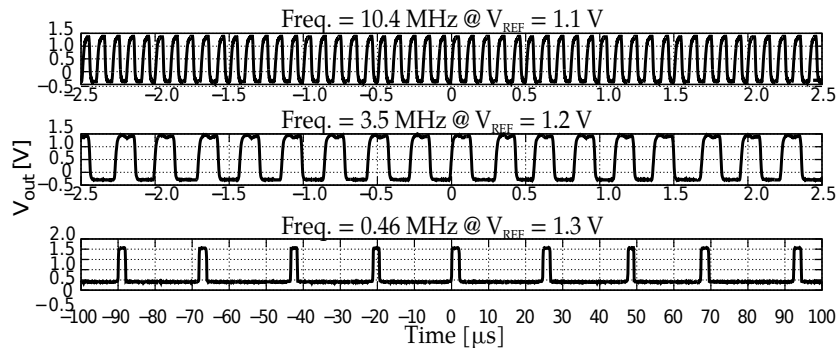


Fig. 26: Sensorless waveforms for the pHCO integrated-circuit obtained from the oscilloscope measurements

Finally, a setup measurement photograph is shown in Figure 25(b). One can observe on the oscilloscope screen, the waveform found applying a 1.3 V of V_{REF} voltage. The signal is digitally-represented denoting for the proper design and operation of buffers. In enlarged view, one can notice the packaged chip fabricated.

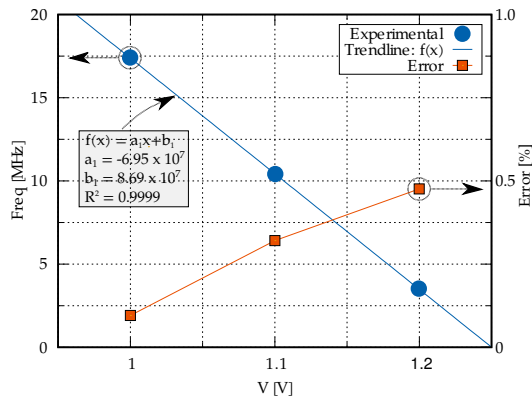


Fig. 27: Performance of the chip sweeping V_{REF} from 1.0 V to 1.2 V

VIII. COMPARISON AMONG STATE-OF-THE-ART WORKS

A brief comparison among some relevant work addressing signal conditioning for ISFET-based sensors is reported in Table VI.

The simulation results reported in our work has presented a lower overall power consumption when compared to works reported in [17] (600 μ W), [20] (230 μ W) and [19] (168.3 μ W), but still larger when compared to works [13] (76 μ W) and [18] (4.5 μ W). Nevertheless, it is important to notice that output signal reported in work [18] is in a current-mode representation, thus afterwards, an ADC may be required for a duly measurement. On the other hand, the AFE silicon area (excluding sensor's area) presented in this work was smaller than all works reported in Table VI, addressing for the circuit simplicity and its prospective use in implantable applications.

The dynamic range (DR) presented in this work (28.24 dB) over the ISFET A conditioning, was higher when compared

to works in [13] (18.32 dB) and [19] (27.7 dB) and lower than others shown in table. In terms of linearity, only works presented in [13] and [19] have reported this figure of merit. The work reported in [13] has found 0.995 of R^2 coefficient, this being only slightly above than the presented in our simulation results. Work reported in [19] has found a 0.5 % of non-linearity error, which also is better than herein reported.

IX. CONCLUSIONS

This paper presented an AFE, designed and fabricated under a 180-nm standard CMOS process, to condition the electrically-weak signal of an ISFET-based sensor directly to digital domain using a pulse frequency modulation technique. Both static and dynamic circuit operation were analyzed and the self-biasing configuration, based on a series-series feedback loop, has been used to tie the ISFET DC operation point.

Post-layout simulations predicted 114.9 μ W and 113.6 μ W of overall power consumption with 0.9866 and 0.9903 of R^2 coefficient for ISFET A and B, respectively. The uppermost linearity error found was 12 % at the pH 10 for both sensors.

Sensorless measurements of the fabricated chip revealed a digitally-represented signal with 0.9999 of R^2 coefficient, 0.47 % of linearity error and about 70 MHz/V of responsivity when applying a voltage ranging from 1.0 V to 1.2 V. The worst-case scenario for the total power consumption was found to be 69.4 μ W, this being inferior to post-layout simulations because of the ISFET absence in the experiment. Moreover, the circuit topology circumvents the body effect problems, suppress the use of OP-AMPs or ADCs, and allows monolithic integration.

X. ACKNOWLEDGMENTS

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¹Digital block: 3.3 V — Analog block: 1.8 V

²Excluding digital and interfacing circuits

³Non-linearity error relative to the linear regression model

Works	[17]	[13]	[18]	[19]	[20]	This work A	This work B
Tech. (μm)	0.18	0.18	0.25	0.35	0.18	0.18	0.18
V_{DD} (V)	2.0	1.8/3.3 ¹	2.5	3.3	1.8	1.8	1.8
Sil. area (mm^2)	≈ 0.4	2.6	-	3	0.036	0.018	0.018
Power (μW)	600	76 ²	4.5	168.3	230	114.9	113.6
ISFET span	0.5-3 V	pH 4-10	5-25 mM	-	-	pH 1-10	pH 1-10
AFE span	0.05-1.9 V	80-200 kHz	50-250 nA	3.6-14.4 nA	-	31-1.2 MHz	39-3.6 MHz
Responsivity	≈ 0.6 V/V	81 kHz/V	10 nA/mM	1.233 and 1.17 nA/mM	27 ns/pH	3.3 MHz/pH	4.4 MHz/pH
Linearity	-	0.5 % ³	-	0.995	-	0.9866	0.9903
DR	72.8 dB	18.32 dB	32.2 dB	27.7 dB	58 dB	28.24 dB	20.69 dB

TABLE VI: Comparison among state-of-the-art works

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