Pedro Emiliano Paro Filho

# A Variable-gain Transimpedance Amplifier for MEMS-based Oscillators

# Um Amplificador de Transimpedância de Ganho Variável para Aplicação em Osciladores Baseados em MEMS

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Universidade Estadual de Campinas
Faculdade de Engenharia Elétrica e de Computação

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Master thesis presented to the School of Electrical and Computer Engineering in partial fulfillment of the requirements for the degree of Master in Electrical Engineering. Concentration area: Electronics, Microelectronics and Optoelectronics.

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Prof. Dr. José Alexandre Diniz (Presidente): _____

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Prof. Dr. Fabiano Fruett: _____

To my parents, Pedro and Melanie, and my grandparents Olivio, Nair, Paula and Kurt

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Se a educação sozinha não pode tranformar a sociedade, tampouco sem ela a sociedade muda.

Paulo Freire

# Abstract

A variable gain Transimpedance Amplifier (TIA) is presented. Realized in 0.18 $\mu$m technology, this amplifier was conceived with the purpose of providing oscillation sustaining for Micro-Electro-Mechanical System (MEMS) based oscillators. Facing a quite challenging trade-off between Gain, Bandwidth, Noise and Power consumption, the TIA was implemented through the cascade of four similar gain stages, with the application of shunt-shunt feedback to lower both input and output resistances. With the employment of a variable-gain stage, this TIA presents a large gain tunability of 53 dB, with a also large maximum transimpedance gain of 118 dB$\Omega$. The circuit simulation also points to a minimum Input-referred Noise Current of 2.51 pA/$\sqrt{}$Hz, and the Replica Biasing method confers a distinct robustness against severe PVT variations. The system also incorporates an Automatic Gain Control (AGC) circuitry to address a poor MEMS Power Handling Capability, and the addition of decoupling capacitors further augments the design applicability. Finally, the obtained transimpedance amplifier is suitable to provide oscillation sustaining for a wide variety of MEMS resonators, and the achievement of an improved noise performance paves the way for a resultant low Phase Noise oscillator.

Key-words: TIA; Transimpedance Amplifier; Variable-gain; AGC; Automatic Gain Control; MEMS resonator; Oscillator; Phase Noise.

# Resumo

Um amplificador de transimpedância (TIA) de ganho variável é apresentado. Implementado em tecnologia 0,18 $\mu$m, o projeto relatado possui a finalidade de prover um amplificador de sustentação para osciladores baseados em ressonadores do tipo MEMS (Micro-Electro-Mechanical System). Entre outros, as peculiaridades de projeto envolvem um desafiante compromisso entre Ganho, Largura de Banda, Ruído e Consumo de potência. Sendo assim, o amplificador foi implementado através do cascateamento de quatro estágios de ganho similares, lançando-se mão de realimentação do tipo shunt-shunt para diminuir as impedâncias de entrada e saída. Através do emprego de um estágio de ganho variável, uma alta faixa dinâmica de ganho é alcançada (53 dB), com um ganho máximo de transimpedância de 118 dB$\Omega$. Além disso, uma baixa corrente de ruído referenciada à entrada é obtida (2,51 pA/$\sqrt{}$Hz), e o método de polarização por réplica atribui uma alta robustez ao sistema nas mais severas variações de processo, tensão de alimentação e temperatura (PVT). O sistema também incorpora um mecanismo de Controle Automático de Ganho (CAG) devido a uma baixa capacidade de potência típica dos dispositivos MEMS, e o uso de capacitores de desacoplamento aumenta ainda mais a aplicabilidade do projeto. Sendo assim, o amplificador de transimpedância obtido pode ser aplicado conjuntamente a uma ampla variedade de ressonadores MEMS, e o baixo parâmetro de ruído alcançado torna possível que o oscilador resultante apresente uma boa performance em termos de ruído de fase.

Palavras-chave: TIA; Amplificador de Transimpedância; Ganho Variável; CAG; Controle Automático de Ganho; Ressonador MEMS; Oscilador; Ruído de Fase.

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# Acronyms

| | |
|---|---|
| AGC | Automatic Gain Control |
| AM | Amplitude Modulation |
| BW | Bandwidth |
| CG | Common-Gate |
| CMF | Common-mode Feedback |
| CMOS | Complementary Metal Oxide Semiconductor |
| CPA | Current Pre-Amplifier |
| $f_{anti}$ | Anti-resonant frequency |
| $f_{res}$ | Resonant frequency |
| FoM | Figure of Merit |
| GBW | Gain-Bandwidth Product |
| GSM | Global System for Mobile communications |
| HSDPA | High Speed Downlink Packet Access |
| IC | Integrated Circuit |
| MEMS | Micro-Electro-Mechanical System |
| MOS | Metal Oxide Semiconductor |
| NMOS | N-type MOS |
| OFDM | Orthogonal Frequency-Division Multiplexing |
| PMOS | P-type MOS |
| PVT | Process-Voltage-Temperature |
| Q-factor | Quality Factor |
| RGC | Regulated Cascode (Boosted-gm) |
| THD | Total Harmonic Distortion |
| TIA | Transimpedance Amplifier |

# Contents

Chapter 1

# Introduction

## 1.1 Goals

The main goal of this thesis is to design an integrated sustaining amplifier for MEMS-based Oscillators. Considering typical resonator's characteristics, the amplifier should provide a large transimpedance gain, with considerable bandwidth. Further requirements include a reduced Input-referred noise current, and lowered input and output resistances. At last, for a wider applicability, the design should present some gain tuning capability, combined with an Automatic Gain Control mechanism.

## 1.2 Motivation

Oscillators are everywhere.
As their most common application, every digital circuit (from thumb drives to microprocessors) needs some sort of time-reference (or 'clock') to synchronize its operations. Moreover, working as frequency references, oscillators represent a critical block of any radio transceiver, significantly affecting its performance, size and cost [1].

However, it is integrating wireless communication systems that these blocks find their most demanding application. In this case, the constant demand for higher transmission data-rates not only represents an increase in system complexity, but also defines tough requirements regarding the oscillator performance [2]. Along with a superior stability over both time and temperature, the oscillator key features must include a high absolute frequency accuracy, and a distinguishable

spectral purity [3], translated into a low Phase Noise.

Due to its relevant impact on system performance, Global System for Mobile Communications (GSM) and standards based on Orthogonal Frequency-Division Multiplexing (OFDM), rely on stringent phase noise parameters to achieve their specifications [4]. For instance, the High-Speed Downlink Packet Access (HSDPA) standard, requires the quite challenging close-to-carrier and far-from-carrier phase noises of -83 dBc/Hz [5] and -132 dBc/Hz [6], respectively. Furthermore, since most of these wireless communication systems are aimed for mobile applications, the claim for increasingly smaller and energy efficient devices also places hard constraints on the oscillator's form factor, power consumption and assembly cost.

In other words, the challenge is to deliver a high performance oscillator, which should also be cheap, small and consume very low power.

In this sense, considering its significantly improved phase noise performance [7], Harmonic oscillators are widely employed in frequency synthesis applications. They are usually implemented as the combination of a resonant structure (defining the oscillation frequency with a high selectivity) and a sustaining amplifier to start-up and maintain oscillation. Both entities have a strong impact on the system behavior, but a few particular resonator's characteristics mostly contributes for a improved phase noise performance, namely a high Quality Factor and large Power Handling Capability [2].

Until very recently, only quartz crystals were capable of achieving such high demands and, combined with their superior stability and absolute frequency accuracy, over the past decades they were the preferred type of resonator to be employed [1]. Nevertheless, among off-chip components used in wireless communication systems, this kind of resonator represents one of the most difficult devices to miniaturize and integrate on chip [8]. Furthermore, quartz crystals' fabrication processes are inherently incompatible with standard CMOS, which represents another relevant drawback to be considered.

For all these aspects, on-chip electrical resonators provided by conventional integrated circuit technologies can be very appealing. These resonators can be fully-monolithic [9], and also offer the advantages of a low cost and a reduced sensitivity to packaging parasitics [10]. However, due to inevitable losses from series resistances, common topologies cannot achieve Quality factors higher than a few tens [9][10], which is prohibitively low considering the intended application.

Even though some effort has been put throughout the years to reduce the parasitics [10],

the increased interconnection resistance offered by standard technologies, makes the design of high-quality inductor coils more difficult [11].

In turn, combining both small size, high Q-factor and increasingly power handling capability, Micro-Electro-Mechanical System (MEMS) resonators has arisen as an interesting alternative over the past decade [12].

From RF switches [13] to a wide variety of sensors [14][15], many MEMS-based devices and systems have been reported in literature. Due to a rapid growth of micro-machining technologies, these devices can now be merged with conventional ICs, allowing MEMS resonators to be integrated in fully-monolithic oscillators, as seen in [2][10][16]. Additionally, low temperature Post-CMOS processing have enabled the fabrication of these devices on top of the active circuitry [17], saving area and reducing the impacts of parasitic bondpads.

In all other cases, where post processing or monolithical integration is not possible, MEMS resonators are yet small enough to be integrated in the same package [16], and either way, the use of such devices represents a drastic reduction in the overall system footprint. As a matter of fact, as mentioned in [16], the use of MEMS technologies offers not only a reduced form factor, but all the benefits of using integrated devices instead of discrete components, like batch processing, higher reliability and reduced use of materials.

As a result, from capacitive to piezoelectrically actuated resonators, a wide variety of MEMS resonators have been reported with different trade-offs in Quality factor, power handling capability and motional resistance. Some of them were even capable of achieving Q factors as high as 180000 [18].

All these achievements, together, made of MEMS resonators a strong competitor to their crystal counterparts, but yet with a few drawbacks to be addressed. The most important aspect is related to a high insertion loss, mainly due to a low electrostatic transduction efficiency [19], modeled as a high motional resistance. Even though considerable progress has been made already [20], high Quality factor MEMS resonators are still reported as achieving motional resistances as high as 880 k$\Omega$ [21], while the crystals' motional resistance ranges from 25 to 200 $\Omega$. This high motional resistance, in turn, has a great impact on the sustaining amplifier design.

Known as Barkhausen criteria [22], there are two basic requirements that must be fulfilled in order to obtain a sustainable oscillation. The first one addresses the loop-gain, that has

to be equal to unity, representing that all sources of loss inside the loop are undertaken by a correspondent amount of gain (given by the sustaining amplifier). The second requirement, in turn, regards the phase shift around the loop, which has to be ideally zero (or as close to zero as possible) at the resonant frequency. As a result, taking into account the high insertion loss mentioned before, for the system to oscillate the sustaining amplifier not only has to provide a large amount of gain, but also a very large bandwidth.

To ease the oscillator design, the motional resistance can be lowered by either decreasing the resonator's transduction gap, or increasing its bias voltage. However, there is a trade-off involved. While the latter reduces the design applicability and increases the system complexity, the former decreases the device's linearity and power handling capability. With a lower power handling capability, MEMS resonators exhibit significant non-linearities even below their maximum drive level [23], which severely affects the system's output phase noise [24].

In this case, the employment of an Automatic Gain Control (AGC) circuitry is strongly recommended [25]. Controlling the output oscillation amplitude, it is possible to avoid the system phase noise degradation by ensuring that the resonator remains vibrating within its linear region. Additionally, in order to prevent the decrease of the resonator's Quality factor through loading effects, it is also important that the sustaining amplifier presents a low input and output resistances [2]. Finally, since the sustaining amplifier noise also affects the oscillator's phase noise, it is also important that this block is properly designed for minimum noise contribution [26].

In summary, to obtain a high performance MEMS-based oscillator, the correspondent sustaining amplifier should provide considerably large gain (at least a few times higher than the resonator's motional resistance) with a very large bandwidth, so minimum phase shift is observed around the resonant frequency. It should also provide reasonable gain controllability, not to affect the system phase noise performance, while presenting both low input-referred noise and terminal resistances. These aspects altogether, make the design of such sustaining amplifier a very challenging task, to be described in the following chapters.

## 1.3 Organization

The remainder of this thesis is organized as follows:

Chapter 2 provides a system overview of the intended oscillator. A top level description is made, briefly enumerating the blocks that together comprises the sustaining amplifier. Later, the most important issues regarding the design and operation of a low phase noise oscillator are addressed, considering typical characteristics of high Quality Factor MEMS resonators from literature. Based on the expected performance, minimum values are specified for the sustaining amplifier parameters.

Chapter 3 describes the design itself, with preliminary analysis of the most commonly applied topologies. Chapter 4 presents the results, with the respective discussions. A results summary table is provided at the end of the chapter, situating the resultant sustaining amplifier among similar state-of-art designs.

Finally, conclusions are drawn on Chapter 5.

Appendix A and B respectively provides: A) the Design Layout and B) a paper related to the presented design.

Chapter 2

# System Specification

The design herein reported comprises a transimpedance amplifier conceived to provide oscillation sustaining for MEMS-based oscillators.

In order to obtain a good performance from the resultant oscillator, the sustaining amplifier should be designed considering specific characteristics of the MEMS resonator, to be known.

## 2.1 MEMS Resonator

As many others, a MEMS resonator consists of a physical system whose behavior may be represented by the following diagram, seen in Figure 2.1.

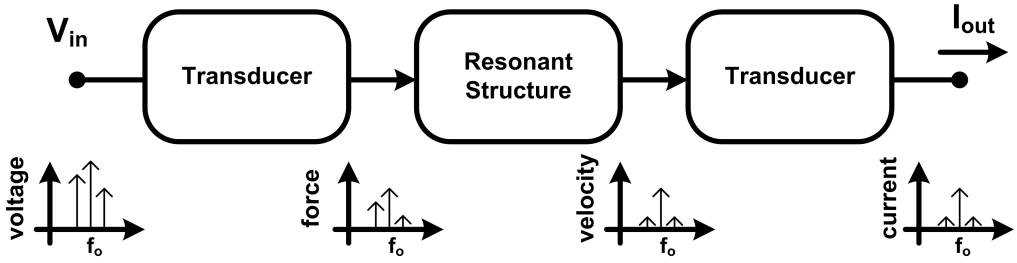



Figure 2.1: Diagram representing MEMS resonator operating principle.

Regardless the transduction method used (which can be either piezoelectric or capacitive), when a input voltage is applied, it is converted into a force in the mechanical domain. This force induces a displacement in the resonant structure that, due to intrinsic characteristics of the substrate and the moving part, turns out acting as a filter, attenuating every frequency

component different from its resonant frequency $f_o$. With ideally only one frequency tone, the structure's velocity is transduced back to the electrical domain as an output current, which can be amplified and fed back in phase with the stimuli that first generated the mechanical displacement. By this means, sustainable motion can be achieved, and an oscillator can be obtained.

Acting as a filter, the resonant structure deeply affects the system behavior, and characteristic parameters such as Quality factor, insertion loss and power handling capability are crucial to determine the resultant oscillator performance [2].

Considering the amplifier design, the insertion loss is by far the most important parameter to be taken into account. Modeled as the resonator's motional resistance, it defines (at resonance) the ratio between the applied input voltage $V_{in}$ and the sensed output current $I_{out}$ (seen in Figure 2.1). As a result, it also determines the amount of gain to be provided by the sustaining amplifier.

As mentioned in [8], the device's motional resistance (as well as the resonant frequency, Quality factor and Power Handling Capability) is a strong function of both device's geometry and bias voltage. However, as a bias voltage increase often demands further circuitry (impacting on the design complexity), a motional resistance reduction through resonator's geometry modifications strongly affects the device's Power Handling Capability, which is another relevant parameter to be considered.

Due to a poor Power Handling Capability, the non-linear behavior of the resonator at increased power levels generates an unexpected $1/f^3$ phase noise component that deeply affects the system performance [25]. For most of the reported designs, that was the main cause that prevented the resultant oscillators to meet the phase noise requirements [27].

The Quality factor, at last, comprehends a valuable Figure of Merit to assess the resonator frequency selectivity. It is generally considered as an empirical parameter, and is mainly determined by the amount of energy lost by the resonant structure either to the substrate (through mechanical coupling) or to environment (through fluidic damping mechanisms [2]).

### 2.1.1 Model

Just like its crystal counterparts, the MEMS resonator can be electrically modeled by the 5-parameter model shown in Figure 2.2.

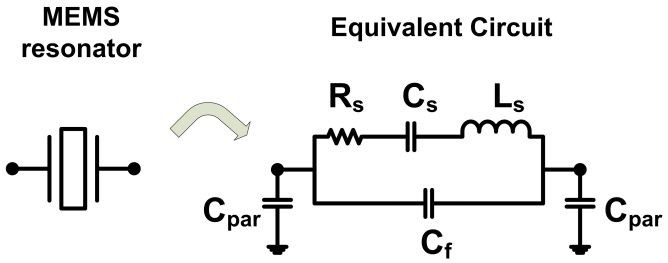



Figure 2.2: MEMS resonator: Equivalent circuit.

This model is mainly consisted of two arms in parallel: the "static arm", represented by the feed-through capacitance $C_f$; and the "motional arm", represented by the series combination of $R_s$, $C_s$ and $L_s$. Named motional resistance, motional capacitance, and motional inductance, respectively, the series components are the most representative elements of the equivalent model. While $R_s$ stands for the already mentioned resonator's motional resistance, it is the combination of the motional capacitance and motional inductance that actually defines the device's resonant frequency, given by Equation 2.1.

$$\omega_{res} = 2\pi f_{res} = \frac{1}{\sqrt{L_s \cdot C_s}} \tag{2.1}$$

The feed-through capacitance $C_f$, in turn, is responsible for creating a so-called "anti-resonant" frequency ($f_{anti}$), which represents the frequency where the equivalent resonator admittance is minimum (Equation 2.2).

$$\omega_{anti} = 2\pi f_{anti} = \sqrt{\frac{C_s + C_f}{L_s \cdot C_s \cdot C_f}} = f_{res} \cdot \sqrt{1 + \frac{C_s}{C_f}} \tag{2.2}$$

Finally, the fifth model parameter $C_{par}$ was included to represent the interconnection parasitic capacitance, seen from each resonator terminal to ground. In the case of MEMS resonators, this capacitance can achieve values as high as 1 pF, which may strongly affect the system bandwidth.

Altogether, the frequency response of a typical MEMS resonator can be seen in Figure 2.3(a).

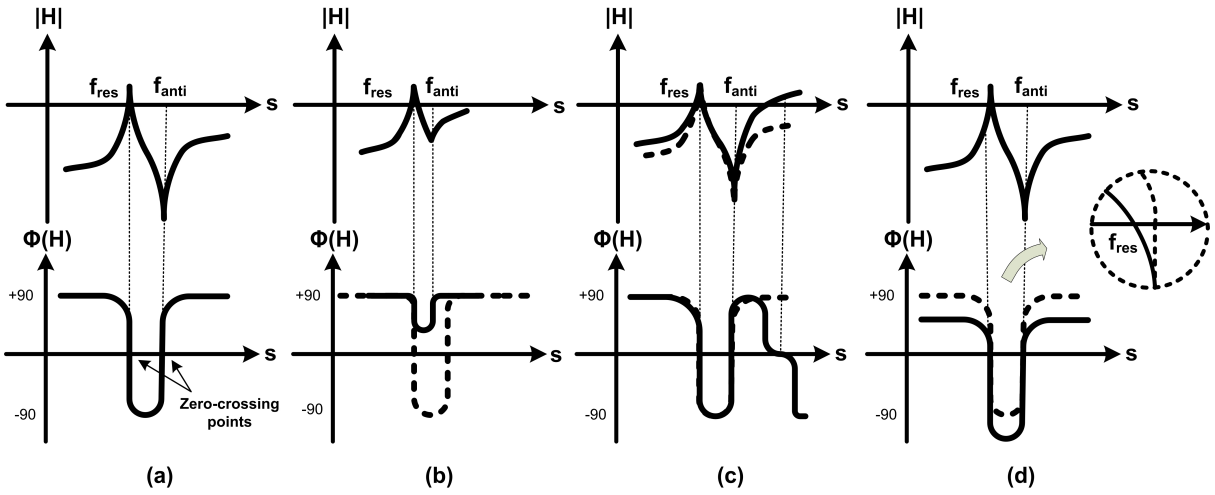



Figure 2.3: Frequency response (a) in typical situation, (b) no zero-crossing due to high feed-through capacitance, (c) higher frequency oscillation and (d) frequency sensitivity increase. The bold dotted line represents the typical gain and phase transfer functions.

As noted, in the phase transfer function two zero-crossing points can be seen. For reasons that will be further made clearer (Section 2.3.1), oscillation can only be achieved if at least unity gain is observed at these zero-crossing frequencies. Hence looking into the impact of the feed-through capacitance into more detail, two problems can be foreseen:

If $C_f$ is too large, the anti-resonant frequency comes closer to $f_{res}$, and the phase transfer function may not cross the zero line anymore, killing any chance of oscillation (Figure 2.3b). Secondly, acting as a zero in the transfer function, a large $C_f$ may lead the system to oscillate at higher frequencies, in which the sustaining amplifier still present positive gain, and the phase transfer function also crosses zero degrees, as shown in Figure 2.3c.

For all these reasons, very special care should be taken to assure a reduced feed-through capacitance. Furthermore, when the phase transfer function of the entire system is considered, two other issues come to play.

When high Q-factor resonators are employed, if the sustaining amplifier phase contribution shifts the zero-crossing point to frequencies where there is not enough gain, the system will not oscillate (Figure 2.3d). Moreover, by adding or subtracting phase shift across the loop, the frequency sensitivity is also increased. A qualitative explanation would be that, for large phase shifts, the zero-crossing frequency starts sitting at a smaller slope region of the phase transfer function, as detailed in Figure 2.3d.

As a result, all these aspects should be taken into account to accomplish a stable oscillation, since it not only concerns the resonator itself, but also the sustaining amplifier and the parasitics involved.

## 2.2 System Overview

In light of the MEMS characteristics above mentioned, the entire system can now be examined.

As shown in Figure 2.4, the oscillator can be represented as the combination of a sustaining amplifier, in closed-loop with the resonator.

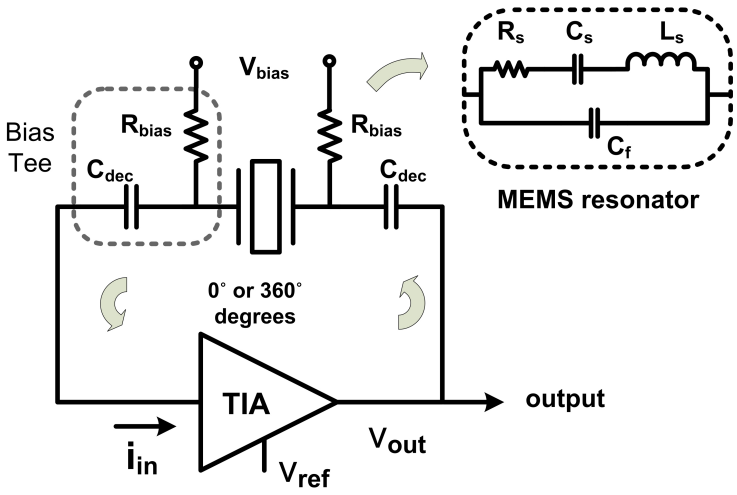



Figure 2.4: Top-level schematic of the MEMS-based oscillator.

However, to increase the transduction efficiency, a large body of reported high Q-factor MEMS resonators present considerable high bias voltages, sometimes as high as incredible 75 volts [28]. These voltage levels are not compatible with MOS technologies, and may cause irreversible damage to the system circuitry. Therefore, to DC decouple the sustaining amplifier from the increased bias voltage, a pair of bias tees was applied, as also seen in Figure 2.4.

Since the sustaining amplifier provides a voltage output in correspondence to a current input, it is named Transimpedance Amplifier (TIA) and, as shown in Figure 2.5, it consists of three different blocks, namely a Variable-gain Amplifier, a Peak Detector and a Comparator.

The latter two blocks comprises the Automatic Gain Control (AGC) circuitry, working in closed loop with the amplifier chain. Through the application of a gain control scheme, it is

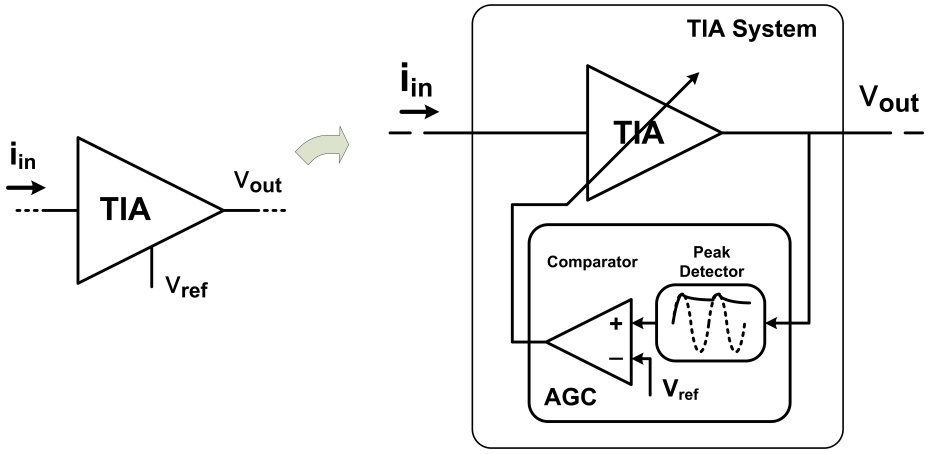



Figure 2.5: Transimpedance Amplifier in detail. A variable Gain Transimpedance Amplifier, a Peak Detector and Comparator comprises the TIA System. The AGC circuitry determines the system gain so the output amplitude equals $V_{ref}$.

possible to optimize the output oscillation amplitude, still keeping the resonator vibrating in its linear region.

Therefore, with the addition of the decoupling capacitors ($C_{dec}$), the system becomes very flexible, fitting a wide variety of resonators, with different combinations of bias voltages and motional resistances. This is a very relevant feature of the proposed design.

Since the design of a resonator is out of scope, few consolidated and state-of-art MEMS devices were considered to define the sustaining amplifier specifications. Finally, the TIA system (including the decoupling capacitors) was designed, simulated and implemented on silicon using the XFAB 0.18 $\mu$m technology.

## 2.3 Oscillator

### 2.3.1 Barkhausen Criteria

As noted in Figure 2.6, the oscillator system can be seen as a positive-feedback system with no external input.

As such, in order to be able to start and sustain oscillation autonomously, both requirements seen in Equation 2.3 should be observed.

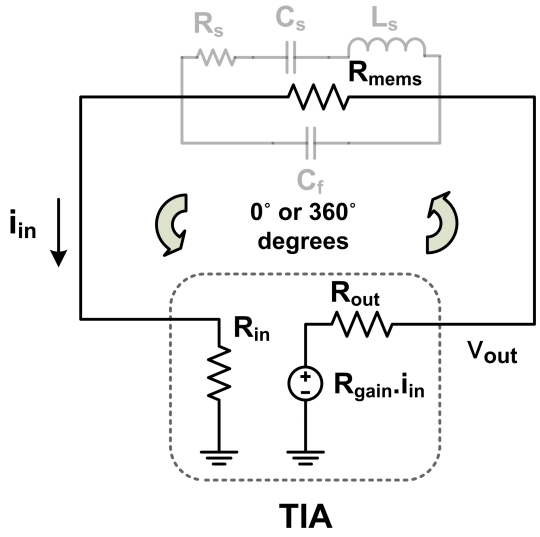



Figure 2.6: Top-level schematic depicting the circuit elements considered in the Barkhausen Criteria. At resonance, $R_{mems} = R_s$.

$$\begin{cases} |H(s)| = 1 \\ \angle H(s) = 0^\circ \; or \; 360^\circ \cdot n, \quad n = 0, 1, 2... \end{cases} \tag{2.3}$$

Known as Barkhausen Criteria, it determines the conditions for any linear system with feedback to attain oscillation and, in this case, it can also be translated as:

i) The transimpedance gain provided by the sustaining amplifier should be equal to (or larger than) the total amount of loss observed in the feedback loop at resonant frequency, given by:

$$R_{gain} \geq R_{tot} = R_{mems} + R_{in} + R_{out}$$

where $R_{mems}$, $R_{in}$ and $R_{out}$ respectively denotes the resonator motional resistance and the sustaining amplifier's input and output resistances.

ii) The total phase shift around the loop, which includes both resonator's and sustaining amplifier's phase contribution, should be in module as close to zero degrees as possible.

As described in [29], these two conditions are necessary, but not strictly sufficient to ensure oscillation in every temperature and process condition. Therefore, a loop gain of at least twice or three times the required value is typically chosen [22].

### 2.3.2 Phase Noise

Once the loop is closed, any noise source (e.g. Thermal noise) from the system will be amplified by the transimpedance amplifier, and filtered by the resonator. If the required conditions stated by the Barkhausen Criteria are met, the positive feedback will increase the signal amplitude and oscillation will start to build.

However, after a specific oscillation amplitude, non-linearities from the resonator and the sustaining amplifier equals the loop gain to unity, by either increasing $R_{mems}$ or reducing $R_{gain}$, respectively. As mentioned before, a fundamental difference between MEMS resonators and their crystal counterparts is their power handling capability.

While Crystal-based oscillators have their oscillation amplitude limited by non-linearities exerted by the sustaining amplifier, MEMS oscillators are limited by their resonator's [2]. As a result, when these non-linearities are expressed, part of the oscillator signal power is spread out along the spectrum, contributing to the overall system noise.

Known as Phase Noise, it severely degrades the performance of wireless communication systems [3] and, in the digital domain, it expresses itself by introducing some kind of uncertainty in the signal's switching instants (also called 'jitter') [30].

A simplified model for Phase-noise spectral density is derived in [31] and, for the system shown in Figure 2.4, the phase noise density-to-carrier power ratio (at offset $f_m$) is given by Equation 2.4 [8].

$$L\{f_m\} = \frac{2kT \cdot (1 + F_{ramp})}{P_o} \cdot \left(\frac{R_{tot}}{R_{mems}}\right) \cdot \left[1 + \left(\frac{f_o}{2 \cdot Q_l \cdot f_m}\right)^2\right] \tag{2.4}$$

where $k$ is the Boltzmann's constant, $F_{ramp}$ the noise contribution factor of the sustaining amplifier and $P_o$ the oscillator signal power.

The factor $Q_l$ represents the loaded Quality factor, given by Equation 2.5

$$Q_l = \frac{R_{mems}}{R_{mems} + R_{in} + R_{out}} = \frac{R_{mems}}{R_{tot}} \tag{2.5}$$

Seen in Equation 2.4, in addition to both large resonator's Quality factor and power handling capability (which increases the output power $P_o$), a low phase noise operation is guaranteed by also decreasing, as much as possible, the noise contribution from the sustaining amplifier (here represented by the noise factor $F_{ramp}$). Moreover, to keep the Quality factor as high as possible,

all the other impedances inside the loop should also be reduced to their minimum. While a low noise contribution is achieved by designing the TIA with a minimum Input-referred noise current, a low Quality Factor degradation is accomplished by making its input and output resistances as low as possible. Those requirements should also be accounted.

## 2.4 TIA Specification

To determine the sustaining amplifier specifications, the schematic shown in Figure 2.7 was considered.

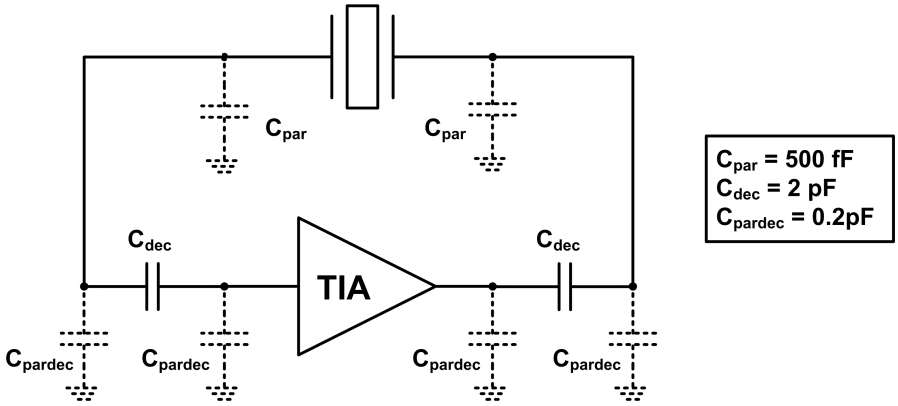



Figure 2.7: Oscillator schematic with parasitics included.

Due to their impact on the system's bandwidth, all relevant elements in the feedback loop were considered, including the parasitics from layout and interconnections. Therefore, to keep on the safe side, during design simulation both sustaining amplifier terminals were loaded with interconnection parasitic capacitances of 500 fF each, and every internal node was loaded with 50 fF to account the phase degradation due to parasitic capacitance expected from layout.

Considering the gain parameter, since motional resistances as high as 79 kΩ was reported in literature [32], to ensure oscillation in every process and temperature condition, the transimpedance gain was chosen to be 200 kΩ.

For the phase condition, to provide a fairly large bandwidth and thus guarantee a low phase shift contribution, all system poles should be sitting at least one decade above the frequency of interest [8]. As a result, in module less than 10 degrees of phase shift would be observed around the resonant frequency, hence meeting the oscillation requirements, and still assuring a low frequency sensitivity (Section 2.1.1).

For the reasons previously mentioned, the amplifier's input and output resistances are another important parameter to be defined. Therefore, to shift the input and output poles to frequencies higher than 500 MHz, the input and output resistances should be kept below 500 Ω.

In turn, the Input-referred Noise was determined considering similar designs and, to achieve a stringent Phase Noise parameter [1], it was dimensioned to be lower than 10 pA/$\sqrt{}$Hz.

All these factors, together, point to a very large gain and bandwidth sustaining amplifier which, in turn, can only be achieved with the expense of considerable power. However, power consumption is another specification parameter to be optimized and, considering also other similar sustaining amplifiers [1][33], it was determined to be made lower than 1 mW.

Finally, for a wide applicability, all the above specified TIA parameters (summarized in Table 2.1) should be observed for resonant frequencies up to 20 MHz.

Table 2.1: System Specification Summary.

| TIA Specifications | |
|---|---|
| Gain | $>$ 106 dBΩ (200 kΩ) |
| \|Phase Shift\| @ 20 MHz | $<$ 10 degrees |
| $R_{in}$,$R_{out}$ | $<$ 500 Ω |
| Input-referred Noise | $<$ 10 pA/$\sqrt{}$Hz |
| Power Consumption | $<$ 1 mW |

Chapter 3

# Design

## 3.1 Literature Overview

Before the circuit design, an extensive research was performed to define the state-of-art in MEMS-based oscillators, and determine the topology that could best fit the design specificities.

From optical communication systems to sensor read-out circuitry, every TIA implementation targets a high Gain-Bandwidth Product (GBW), and many techniques were proposed with this purpose [34]. However, considering the specific application of MEMS-based oscillators, by far the preferred approach to enhance the circuit's GBW is the employment of Common-Gate (CG) (Figure 3.1) input stages [35][36] (and their improved form known as Boosted-gm Regulated Cascode (RGC) [37][38]).

As mentioned in [22], these topologies are known for their well-behaved time response, with the special feature of providing lower input resistances.

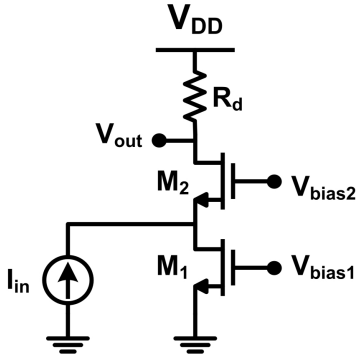



Figure 3.1: Common-Gate Topology [22].

$$R_{in\,CG} = \frac{g_d + g_{ds2}}{g_d \cdot (g_{m1} + g_{ds1} + g_{ds2}) + g_{ds1}g_{ds2}}$$
$$= \frac{R_d + r_{ds2}}{1 + g_{m2}r_{ds2}} \parallel r_{ds1}$$
$$\approx \frac{1}{g_{m2}} \tag{3.1}$$

where $g_{mx}$ and $g_{dsx}$ denotes the transconductance and drain-source conductance of transistor $M_x$, respectively, and $g_d$ represents the load conductance, given by $g_d = 1/R_d$.

Derived from Figure 3.1, the Equation 3.1 demonstrates that the input resistance of a Common-Gate stage can be lowered just by increasing the transconductance of the input transistor. However, this solution comes with a inevitable high power expense if considerably low input resistances are required. This problem, in turn, is partially solved if a common source amplifier is applied in closed loop with the input transistor, resulting in the so-called Boosted-gm Regulated Cascode (RGC) (Figure 3.2).

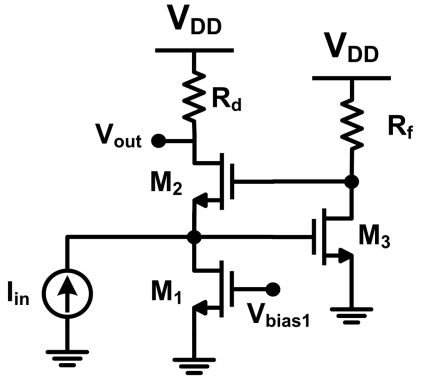



Figure 3.2: Boosted-gm Regulated Cascode Topology [38].

As shown in Equation 3.2, this topology's input resistance is significantly reduced, since it is further divided by a factor equal to the feedback amplifier gain ($g_{m3}R_f$). Nevertheless, if both CG and RGC noise performances are examined, a relevant drawback is revealed.

$$
\begin{aligned}
R_{in\ RGC} &= \frac{1}{\dfrac{g_d}{g_d + g_{ds2}} \cdot \left( g_{m2} \left( 1 + \dfrac{g_{m3}}{g_f + g_{ds3}} \right) + g_{ds2} \right) + g_{ds1}} \\
&\approx \frac{1}{g_{m2}\left(1 + g_{m3} R_f\right)} \parallel r_{ds1} \\
&\approx \frac{1}{g_{m2}\left(1 + g_{m3} R_f\right)}
\end{aligned} \tag{3.2}
$$

By evaluating both topology's input-referred noise currents ($\overline{I^2_{n,in}}$), it can be seen (Equations 3.3 and 3.4) that in both cases the noise currents generated by $M_1$ and $R_d$ are directly referred to the input node with a unity factor, deeply contributing to the system noise.

$$
\begin{aligned}
\overline{I^2_{n,in}}_{\,CG} &= \overline{I^2_{n,in}}\big|_{M_1} + \overline{I^2_{n,in}}\big|_{M_2} + \overline{I^2_{n,in}}\big|_{R_d} \\
&\approx \overline{I^2_{n,R_d}} + \overline{I^2_{n,M_1}}
\end{aligned} \tag{3.3}
$$

$$
\begin{aligned}
\overline{I^2_{n,in}}_{\,RCG} &= \overline{I^2_{n,in}}\big|_{M_1} + \overline{I^2_{n,in}}\big|_{M_2} + \overline{I^2_{n,in}}\big|_{R_d} + \overline{I^2_{n,in}}\big|_{M_3+R_f} \\
&\approx \overline{I^2_{n,R_d}} + \overline{I^2_{n,M_1}}
\end{aligned} \tag{3.4}
$$

Also providing a low input resistance, the employment of current pre-amplifiers (CPA) [1] can be seen as another alternative. Compared to the Common-Gate, this topology has the advantage of providing a larger transimpedance gain, enhanced by a current multiplication given by the aspect ratios between $M_1$ and $M_5$ ($A_i \approx g_{m5}/g_{m1}$).

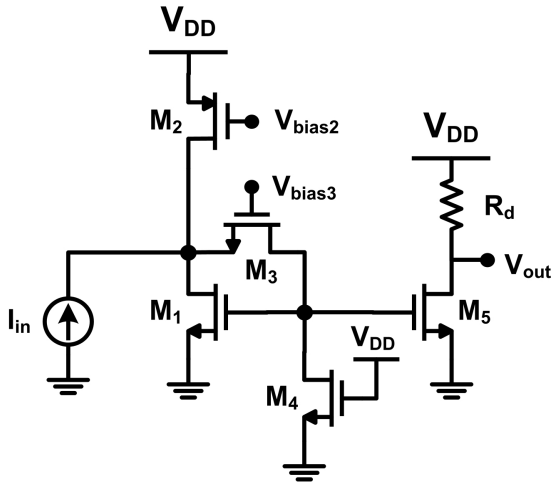



Figure 3.3: Current Pre-Amplifier Topology [1].

$$R_{in\,CPA} = \frac{1}{g_{m1} \cdot \left(1 + \dfrac{g_{m3}}{g_{ds3}}\right) + g_{ds1} + g_{ds2}}$$

$$\approx \frac{1}{g_{m1} g_{m3} r_{ds3}} \tag{3.5}$$

With a total transimpedance gain of $R_{gain_{CPA}} \approx g_{m5}/g_{m1} \cdot (R_d \parallel r_{ds5})$, the shunt feedback provided by $M_3$ further reduces the input resistance of the current pre-amplifier, as seen in Equation 3.5. However, as confirmed by Equation 3.6, just like the Common-Gate-based topologies, the current noise given by transistors $M_1$ and $M_2$ are also coupled directly to the input node with a unity factor.

$$\overline{I^2_{n,in}}_{\,CPA} = \overline{I^2_{n,in}}\big|_{M_1+M_2} + \overline{I^2_{n,in}}\big|_{M_3+M_4} + \overline{I^2_{n,in}}\big|_{M_5+R_d}$$

$$\approx \overline{I^2_{n,M_1}} + \overline{I^2_{n,M_2}} + ... \tag{3.6}$$

As a result, both Boosted-gm Regulated Cascode and Current Pre-Amplifier topologies may present prohibitively high input-referred noise currents, and for this reason these topologies were left aside.

In turn, first demonstrated by Razavi in [39], the topology shown in Figure 3.4 represents a significant improvement in terms of noise performance. Seen in Equation 3.7, the noise generated by the amplifier becomes dominant only at higher frequencies, while the midband input-referred noise is dominated by the $R_d$ contribution, which is attenuated by the current gain $A_i = (1 + C_2/C_1)$ [39].

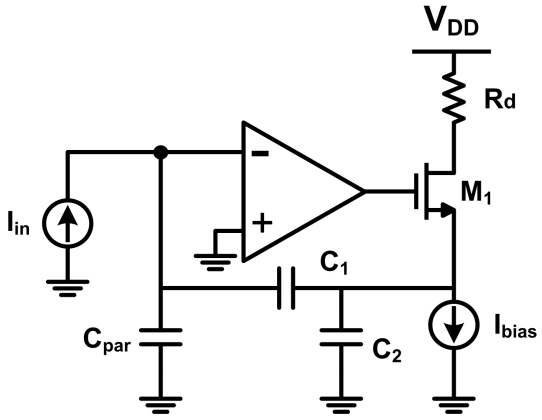



Figure 3.4: Capacitive Feedback TIA Topology [39].

$$\overline{I_{n,in}^2}_{\,Razavi} = \frac{\overline{I_{n,R_d}^2}}{|A_i|^2} + \overline{V_{n,\,Amp}^2} \cdot \omega^2 \left(C_1 + C_{par}\right)^2$$

$$\approx \frac{\overline{I_{n,R_d}^2}}{\left(1 + \dfrac{C_2}{C_1}\right)^2} \tag{3.7}$$

Another benefit of this topology is that a large transimpedance gain can be easily achieved with good precision, since its gain is determined by the ratio of two capacitors ($C_2/C_1$). However, for the same reason, this topology becomes very interesting only for fixed-gain transimpedance amplifiers.

The manipulation of the capacitance ratio through the application of an AGC circuitry, not only proved to be difficult, but also a small gain tunning range could be achieved.

Finally, with a relaxed noise performance and a very straightforward implementation, the shunt-shunt feedback TIA was evaluated as the most suitable topology for the required specifications. With a simplified representation shown in Figure 3.5, the shunt-shunt topology has

the input-referred noise current given by Equation 3.8.

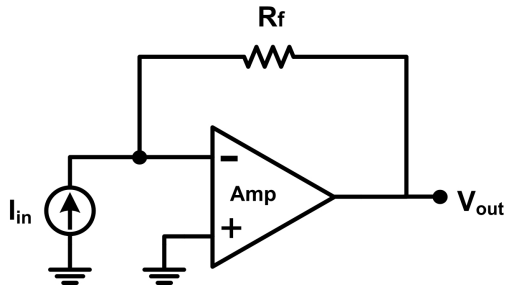



Figure 3.5: Simplified schematic of the Shunt-Shunt Feedback Transimpedance Amplifier [22].

$$\overline{I^2_{n,in}}_{sht-sht} = \frac{4kT}{R_f} + \frac{\overline{V^2_{n,Amp}}}{R_f} \tag{3.8}$$

The main advantage of this topology is that, since $R_f$ does not carry significant DC current, it can be maximized to reduce the total input-referred noise current, also increasing the transimpedance gain ($R_{gain_{sht-sht}} \approx R_f$). Furthermore, the required high transimpedance gain can be achieved by cascading similar gain stages. However, their phase shift contributions should be addressed by shifting their poles to higher frequencies. At last, by means of shunt-shunt feedback, the transimpedance amplifier input and output resistances can also be significantly reduced.

## 3.2 TIA Design

### 3.2.1 Shunt-shunt Feedback

Either intentionally or through unwanted parasitics, feedback is present in almost every analog circuit.

Divided into two kinds (positive and negative), the feedback concept is based on measuring the output signal, and feeding it back to the system input. Depending on how the measured signal is fed back (positive for 'in phase', and negative for 'counterphase'), the concept can be either used to obtain a better controllability of the output signal, or to drive the system into oscillation.

While positive feedback is already applied in the oscillator by attending the Barkhausen Criteria (phase condition), the negative feedback can be locally used in the sustaining amplifier to reduce its input and output resistances, and hence increase the system bandwidth. Furthermore, negative feedback also provides gain desensitization against both device aging and parameter changes, which is another relevant benefit.

Considering the intended application, the sustaining amplifier to be designed should provide a voltage output signal in correspondence to a current input. As such, to measure and compare signals of equal nature, two parallel (shunt) connections should be made: The first to measure the output quantity, as a voltmeter, and the second to generate a current subtraction at the input node. Named shunt-shunt feedback topology, it can be represented by the diagram seen in Figure 3.6.

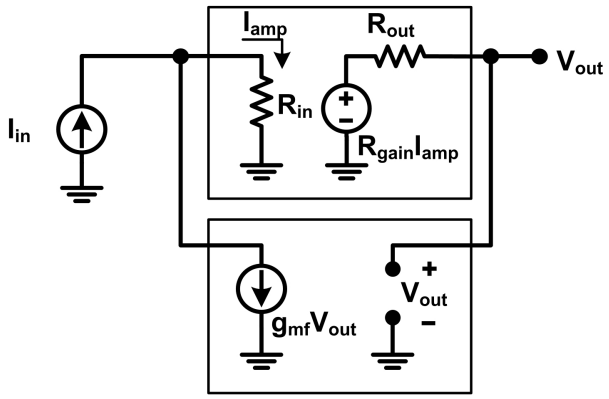



Figure 3.6: Shunt-shunt feedback diagram.

$$\begin{cases} R_{gain\ sht-sht} = \dfrac{V_{out}}{I_{in}} = \dfrac{R_{gain}}{1 + g_{mf} R_{gain}} \approx \dfrac{1}{g_{mf}} = R_f \\ R_{in\ sht-sht} = \dfrac{R_{in}}{1 + g_{mf} R_{gain}} \\ R_{out\ sht-sht} = \dfrac{R_{out}}{1 + g_{mf} R_{gain}} \end{cases} \tag{3.9}$$

As shown in Equation 3.9, the shunt-shunt feedback lowers both input and output resistances by a factor of $(1 + g_{mf} R_{gain})$, and the closed-loop gain is simply given by the feedback resistor $(R_f = 1/g_{mf})$.

### 3.2.2 Variable-gain Transimpedance Amplifier

Seen in Figure 3.7, the sustaining amplifier can be subdivided into three building blocks: the Variable-gain Transimpedance Amplifier, the Bias circuitry and the Automatic Gain Control circuitry.

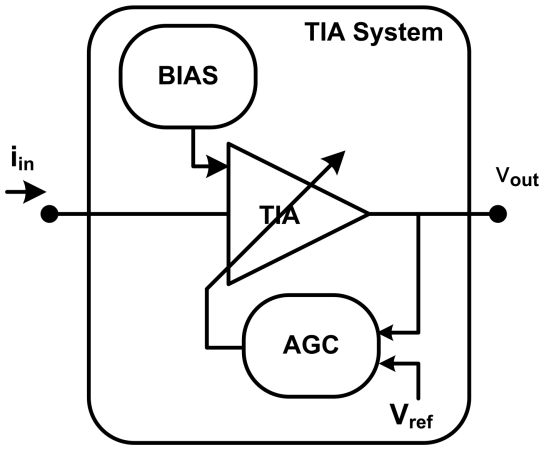



Figure 3.7: Top-level schematic of the proposed Transimpedance Amplifier system.

Once more, the topology to be applied should be able to deliver a large transimpedance gain with a considerably wide bandwidth and, to enhance the system BW and not degrade the resonator Quality factor, both terminal's resistances should be minimized.

For the presented benefits, the amplifier is based on the shunt-shunt feedback topology, and a top-level view of its schematics can be seen in Figure 3.8.

As noted, the variable-gain transimpedance amplifier is consisted of four inverting stages cascaded, with the first and fourth stages in closed-loop. Seen in detail in Figure 3.9, the first inverting stage, with the feedback resistance $R_{var}$, comprises the actual variable-gain stage of the whole amplifier.

Due to the shunt feedback exerted by $R_{var}$, this stage has a lowered input resistance and a straightforward transresistance gain, respectively given by Equation 3.10.

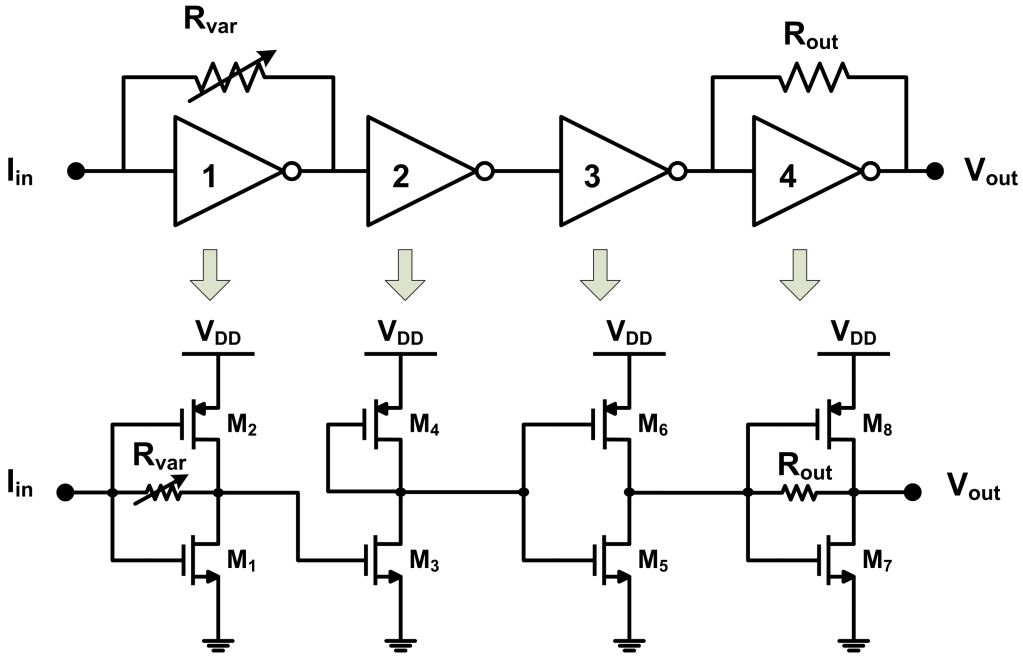



Figure 3.8: Top-level and transistor level schematic of the applied Variable-gain Transimpedance Amplifier topology.

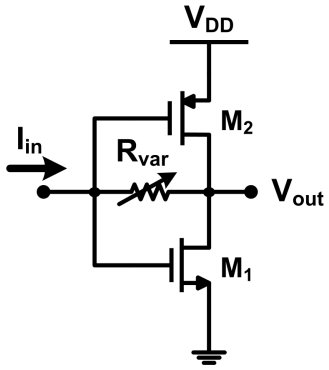



Figure 3.9: Variable-gain first stage.

$$\begin{cases} R_{gain_1} = \dfrac{g_{var} - g_{m_{1,2}}}{g_{var} \cdot \left(g_{ds_{1,2}} + g_{m_{1,2}}\right)} \overset{R_{var} \gg \frac{1}{g_{m_{1,2}}}}{\approx} -R_{var} \\ R_{in_1} = \dfrac{g_{var} + g_{ds_{1,2}}}{g_{var} \cdot \left(g_{ds_{1,2}} + g_{m_{1,2}}\right)} \overset{R_{var} \ll r_{ds_{1,2}}}{\approx} \dfrac{R_{var}}{g_{m_{1,2}} r_{ds_{1,2}}} \end{cases} \tag{3.10}$$

where $g_{m_{1,2}} = g_{m_1} + g_{m_2}$, $g_{ds_{1,2}} = g_{ds_1} + g_{ds_2}$ and $r_{ds_{1,2}} = r_{ds_1} \parallel r_{ds_2}$

As noted, the shunt feedback diminishes the input resistance by a factor equal to the inverter amplifier gain ($A_v = g_{m_{1,2}} r_{ds_{1,2}}$). Furthermore, both $R_{gain_1}$ and $R_{in_1}$ values can be modified by adjusting $R_{var}$ through the control signal $V_{ctrl}$.

The variable resistor $R_{var}$, in turn, was implemented as a NMOS transistor ($R_{mos}$) in combination with a fixed resistance $R_{max}$, seen in Figure 3.10.

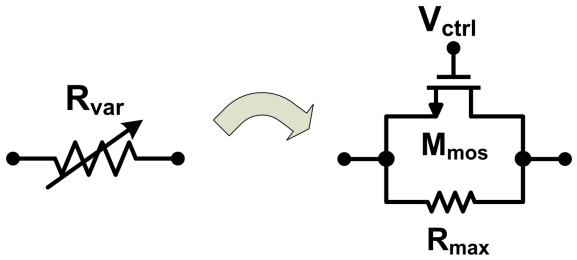



Figure 3.10: $R_{var}$ implementation.

Operating in the triode region, when $M_{mos}$ gate-source voltage ($V_{gs,Mmos}$) becomes higher than the threshold voltage $V_{th}$, the channel is formed and the device's equivalent resistance drops drastically.

$$R_{mos} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs,Mmos} - V_{th})} \tag{3.11}$$

As seen in Equation 3.11, the channel resistance $R_{mos}$ is inversely proportional to $V_{gs,Mmos}$. However, this relationship is non-linear and, for a small control voltage increase, a very large channel resistance variation is observed.

As a result, in order to proper control and set a stable transimpedance gain during steady-state operation, a very large gain AGC circuitry would be necessary. Nevertheless, with the addition of the parallel resistance $R_{max}$, this problem is solved. Through the parallel combination of $R_{mos}$ and $R_{max}$, when $V_{gs,Mmos} = 0$ and $R_{on}$ reaches its maximum value ($> 1$ M$\Omega$), the equivalent resistance equals $R_{max}$. Similarly, when $V_{gs,Mmos}$ is maximum and $R_{mos}$ reaches its minimum value, the equivalent resistance is then given by $R_{mos}$. Varying within a much lower range, the adjustment of the variable resistance $R_{var}$ (and hence the transimpedance gain) is significantly facilitated.

In turn, the provided expression for the equivalent channel resistance (Equation 3.11) only holds for $M_{mos}$ operating in the triode region. As the input node voltage is determined by the bias circuitry (and remains practically constant at $V_{bias}$), in cases when the output excursion of the first stage exceeds the $M_{mos}$ saturation voltage, the NMOS transistor 'saturates' and leaves its linear operation region. As a consequence, the $R_{var}$ resistance increases abruptly, and the gain is no longer controlled by only $V_{ctrl}$.

To avoid this non-linearity, the gain of the first stage was reduced and hence its output swing. However, to achieve the minimum transimpedance gain required by specification, further gain stages had to be included.

With this purpose, the third and fourth stages were added to the amplifier chain (Figure 3.11), with a combined voltage gain given by Equation 3.12.

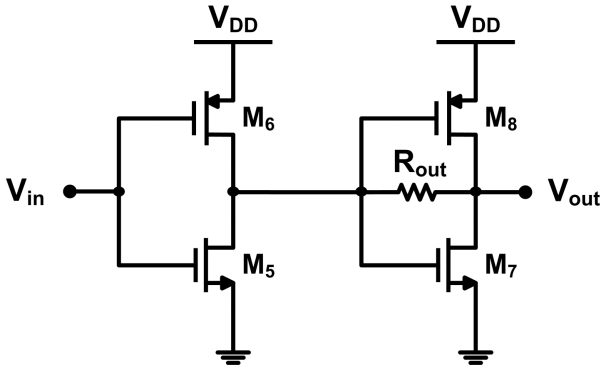



Figure 3.11: Third and Fourth gain stages.

$$A_{v_{3,4}} = \frac{g_{m_{5,6}}}{g_{out} + \underbrace{\frac{\left(g_{out} + g_{ds_{5,6}}\right)\left(g_{out} + g_{ds_{7,8}}\right)}{g_{m_{7,8}} - g_{out}}}_{\approx 0}} \tag{3.12}$$

$$\approx \frac{g_{m_{5,6}}}{g_{out}} = g_{m_{5,6}} R_{out} \tag{3.13}$$

where $g_{out} = 1/R_{out}$.

As shown, the gain expression given by Equation 3.12 can be a lot simplified. Due to the shunt feedback, the input resistance of the fourth stage can be made much lower than the output resistance of the third stage. As a result, since most of the current provided by $M_5$ and $M_6$ flows

directly through $R_{out}$, these two stages in combination can be seen as a single transconductance-transimpedance amplifying stage, with a voltage gain given by $A_{v_{3,4}} = g_{m_{5,6}} R_{out}$. Furthermore, also due to feedback, the output resistance of the fourth stage is also reduced (Equation 3.14).

$$R_{out_{3,4}} = \frac{1}{\left(g_{out} + g_{ds_{7,8}}\right) + \dfrac{g_{out}\left(g_{m_{7,8}} - g_{out}\right)}{g_{out} + g_{ds_{5,6}}}}$$

$$\approx \frac{1}{g_{m_{7,8}}} \tag{3.14}$$

considering that $g_{out} \gg g_{ds_{5,6}}, g_{ds_{7,8}}$.

If the fourth stage output resistance is made low enough, the employment of an output buffer to drive the resonator can be discarded. Considerably reducing power consumption, this aspect represents another relevant feature of the proposed topology.

Additionally, since $R_{out}$ is implemented as a fixed-value integrated resistor, its resistance is not affected by the output voltage swing. As a consequence, the amplifier output is able to swing from almost rail-to-rail, with no impact in linearity (hence achieving a reduced output harmonic distortion - THD).

At last, also integrating the amplifier chain, the second inverter amplifier was included (Figure 3.12). In special, the second stage does not provide voltage amplification (Equation 3.15), but only the necessary phase inversion to achieve the equivalent zero degrees of phase shift at the amplifier output. With $M_4$ connected as diode, the impact of the second stage on the system bandwidth is also reduced.

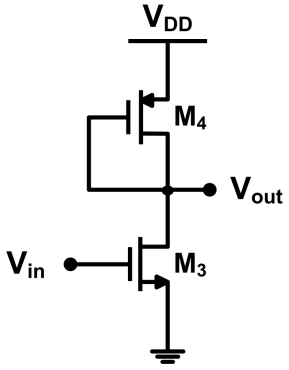



Figure 3.12: Second gain stage.

$$A_{v_2} = \frac{-g_{m_3}}{(g_{m_4} + g_{ds_3} + g_{ds_4})}$$
$$\approx \frac{-g_{m_3}}{g_{m_4}} \tag{3.15}$$

considering that $g_{m_4} \gg g_{ds_3}, g_{ds_4}$.

Accounting all amplifying stages, the overall transimpedance gain at low frequencies is given by Equation 3.16.

$$R_{TIA} \approx R_{gain_1} \cdot A_{v_2} \cdot A_{v_{3,4}}$$
$$\approx R_{var} \frac{g_{m_3}}{g_{m_4}} \, g_{m_{5,6}} R_{out} \tag{3.16}$$

For noise purposes, the first stage's gain was chosen to be the largest, achieving approximately 85dB. The remaining 21dB required by specification was divided between the second and third/fourth stages, with the respective individual contribution of 0dB and 21dB.

When considering the amplifier's frequency response, several factors come into play. Firstly, since large interconnection parasitics are expected ($C_{par} \sim 1pF$), most likely the dominant poles will be located at the amplifier's input and output nodes, contributing in great extent to the overall phase shift. Secondly, every internal node of the amplifier is loaded with parasitic capacitances that also degrades the system bandwidth, either coming from subsequent stages input transistors, or layout routing.

Each inverter stage was sized to present a sufficiently low output resistance, according to the expected amount of load capacitance. As a consequence, each node had its time constant ($\tau_{node}$) made low enough so the overall system's bandwidth could be optimized. Figure 3.13 shows the variable-gain transimpedance amplifier with its respective node time constants. A particular transfer function is evaluated for each gain stage, and the overall frequency response is given by Equation 3.19.

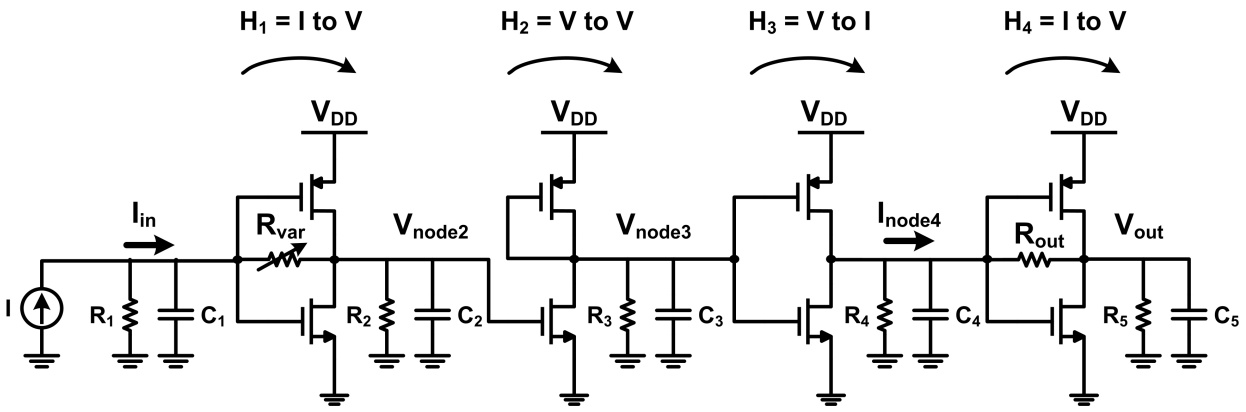



Figure 3.13: Transimpedance amplifier with its respective node capacitances and node resistances.

$$\tau_1 = R_1 \cdot C_1 \qquad \tau_2 = R_2 \cdot C_2 \qquad \tau_3 = R_3 \cdot C_3$$

$$\begin{cases} R_1 = R_{mems} = \dfrac{1}{g_{node_1}} \\ C_1 = C_{par} + C_{gs_{1,2}} + C_{layout} \end{cases} \quad \begin{cases} R_2 = \dfrac{1}{g_{ds_1} + g_{ds_2}} \\ C_2 = C_{gs_3} + C_{layout} \end{cases} \quad \begin{cases} R_3 = \dfrac{1}{g_{ds_1} + \frac{1}{g_{m_4}}} \\ C_3 = C_{gs_{4,5,6}} + C_{layout} \end{cases} \tag{3.17}$$

$$\tau_4 = R_4 \cdot C_4 \qquad \tau_5 = R_5 \cdot C_5$$

$$\begin{cases} R_4 = \dfrac{1}{g_{ds_5} + g_{ds_6}} \\ C_4 = C_{gs_{7,8}} + C_{layout} \end{cases} \quad \begin{cases} R_5 = \dfrac{1}{g_{ds_7} + g_{ds_8}} \\ C_5 = C_{par} + C_{layout} \end{cases}$$

$$H_{TIA} = H_1 \cdot H_2 \cdot H_3 \cdot H_4$$

$$where \quad \begin{cases} H_1 = \dfrac{g_{var} - g_{m_{1,2}}}{\left(g_{var} + g_{node_1}\right)\left(g_{var} + g_{node_2}\right) - g_{var}\left(g_{var} - g_{m_{1,2}}\right)} \\ H_2 = \dfrac{g_{m_3}}{g_{node_3}} \\ H_3 = g_{m_{5,6}} \\ H_4 = \dfrac{g_{out} - g_{m_{7,8}}}{\left(g_{out} + g_{node_4}\right)\left(g_{out} + g_{node_5}\right) - g_{out}\left(g_{out} - g_{m_{7,8}}\right)} \end{cases} \tag{3.18}$$

where $g_{m_{x,y}} = g_{m_x} + g_{m_y}$ and $g_{node_x} = 1/R_x + sC_x$.

$$\therefore H_{TIA} = \frac{g_{m_{3,4}} g_{m_{5,6}} \left(g_{var} - g_{m_{1,2}}\right)\left(g_{out} - g_{m_{7,8}}\right)}{g_{node_3}\left[\left(g_{var}+g_{node_1}\right)\left(g_{var}+g_{node_2}\right) - g_{var}\left(g_{var}-g_{m_{1,2}}\right)\right]\left[\left(g_{out}+g_{node_4}\right)\left(g_{out}+g_{node_5}\right) - g_{out}\left(g_{out}-g_{m_{7,8}}\right)\right]} \tag{3.19}$$

**Transistor Sizing**

At last, all inverting amplifiers were made as scaled copies of the same inverter, and all transistors were sized with the same length and finger width. By keeping a constant N-P ratio (three in this case) and equally scaling their finger numbers at each amplifying stage, every internal node is forced to have the same bias voltage.

Since the transistor transconductance is proportional to the device's aspect ratio, if the finger number is doubled, $g_m$ is also doubled. Moreover, the transconductance increase is accompanied by a decrease in same proportion of the transistor output impedance ($g_{ds}$). As a result, after scaling the intrinsic gain of the inverting amplifier remains the same, but the lower output impedance shifts the output pole to higher frequencies, thus enhancing the system bandwidth.

Therefore, considering the bandwidth specification, every stage was dimensioned to present a convenient trade-off in gain, bandwidth, noise and power consumption. Furthermore, since every node is sitting at the same bias voltage, no DC current is carried by the feedback resistors, so they could be increased to improve the system noise performance.

The bias voltage, in turn, was chosen to sit at mid-rail, so maximum amplitude excursion could be symmetrically observed around the operation point.

### 3.2.3 Bias Replica

A relevant issue concerning high gain amplifiers is their biasing. Small deviations of the bias point (e.g. due to mismatch or supply voltage variations) are also multiplied by the amplifier gain and may drive the latter stages out of the linear operation.

For this reason, the replica biasing method was chosen. It consists in defining the bias voltage by the employment of an exact copy, in closed-loop, of the circuit to be biased. By closing a loop around the replica, the circuitry stabilizes itself at a specific bias point, which can be reproduced at the actual amplifier by sampling its output voltage.

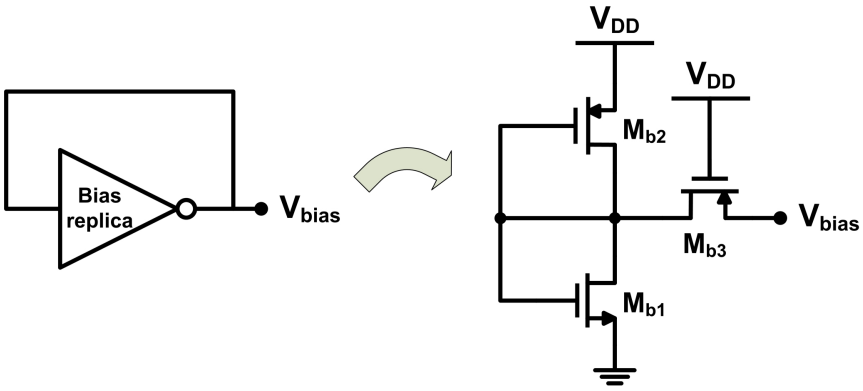



Figure 3.14: Top-level and transistor level schematic of the bias replica.

Compared to the Common-Mode Feedback (CMF) biasing method, it confers the design several advantages in terms of stability and power consumption.

As a replica, improved matching is achieved between the variable-gain amplifier and the bias circuitry. Furthermore, by allowing the bias voltage to dynamically change with process, voltage and temperature (PVT) variations, the amplifier chain is kept stable and the system becomes more robust against disturbances [40].

Interestingly, it is also possible to scale down the replica, with no impact on the bias voltage, reducing both area and power consumption. Moreover, since every internal node of the amplifier was designed to be sitting at the same bias voltage, only one inverting amplifier is sufficient to bias the entire chain.

At last, once the replica is also connected to the input node, a NMOS transistor was employed to cascade the bias circuitry ($M_{b3}$).

### 3.2.4 Noise Analysis

As already mentioned, the shunt-shunt feedback topology was chosen considering its improved performance in terms of noise. More specifically, both feedback resistor and amplifier noise contributions are divided by $R_f$ when referred to input terminal. Therefore, this design component can be increased to optimize the amplifier noise performance.

To provide further insight about the topology, each device's noise contribution was deduced [22] and the input-referred noise power spectral density was evaluated (Equation 3.20).

Represented by the factors $K_{1-6}$, the exercise provides a good assessment of the most critical devices. Moreover, the derivation of Equation 3.20 shows that a better noise performance can be obtained by concentrating most of transimpedance gain in the earlier stages, so the noise contribution of the subsequent stages could be further attenuated.

$$\begin{aligned}\overline{I_{n,in}^2}_{TIA} = &\frac{\overline{I_{n,R_{var}}^2}\cdot|K_1|^2}{|H_1|^2} + \frac{\overline{I_{n,M_{1,2}}^2}\cdot|K_2|^2}{|H_1|^2} + \frac{\overline{I_{n,M_{3,4}}^2}\cdot|K_3|^2}{|H_1\cdot H_2|^2} + \frac{\overline{I_{n,M_{5,6}}^2}\cdot|K_4|^2}{|H_1\cdot H_2\cdot H_3|^2} \\ &+ \frac{\overline{I_{n,M_{7,8}}^2}\cdot|K_5|^2}{|H_1\cdot H_2\cdot H_3\cdot H_4|^2} + \frac{\overline{I_{n,R_{out}}^2}\cdot|K_6|^2}{|H_1\cdot H_2\cdot H_3\cdot H_4|^2}\end{aligned} \tag{3.20}$$

$$where \quad \begin{cases} K_1 = \dfrac{g_{m_{1,2}} + g_{node_1}}{g_{var}\left(g_{m_{1,2}} + g_{node_1} + g_{node_2}\right) + g_{node_1}g_{node_2}} \\ K_2 = \dfrac{g_{var} + g_{node_1}}{g_{var}\left(g_{m_{1,2}} + g_{node_1} + g_{node_2}\right) + g_{node_1}g_{node_2}} \\ K_3 = \dfrac{1}{g_{node_3}} \\ K_4 = 1 \\ K_5 = \dfrac{g_{m_{7,8}} + g_{node_4}}{g_{out}\left(g_{m_{7,8}} + g_{node_4} + g_{node_5}\right) + g_{node_4}g_{node_5}} \\ K_6 = \dfrac{g_{out} + g_{node_4}}{g_{out}\left(g_{m_{7,8}} + g_{node_4} + g_{node_5}\right) + g_{node_4}g_{node_5}} \end{cases} \tag{3.21}$$

### 3.2.5 Automatic Gain Control

Because of a limited power handling capability, non-linearities from the MEMS resonator are exerted at lower power levels. Thereby, to control the oscillation output amplitude and prevent the degradation of the system phase noise performance, an Automatic Gain Control circuitry was implemented. Shown in Figure 3.15, this topology is widely applied [8][40] and consists of a peak detector followed by a comparator to approximate the oscillation amplitude to the expected reference value, given by $V_{REF}$.

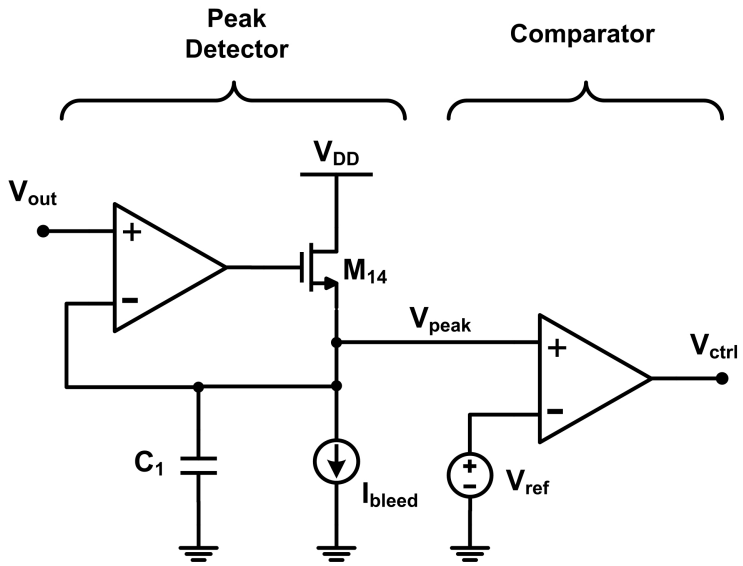



Figure 3.15: Top-level schematic of the implemented Automatic Gain Control circuitry.

After these two operations, the comparator output voltage ($V_{ctrl}$) is fed back to the variable-gain stage, defining the TIA transimpedance gain.

#### Peak Detector

The employed Peak Detector block consists of a peak rectifier with a MOS transistor working as diode in the feedback path. Connected to the output, an integrated capacitor of 1.2 pF samples the signal's peak value, and a bleeding current discharges it.

When $V_{out}$ is higher than $V_{peak}$, the difference between these two voltages is amplified by the operational amplifier, approaching the positive supply voltage ($V_{DD}$) with a high gain. At this moment, $M_{14}$ is switched ON and the sampling capacitor is charged until $V_{peak}$ equals $V_{out}$.

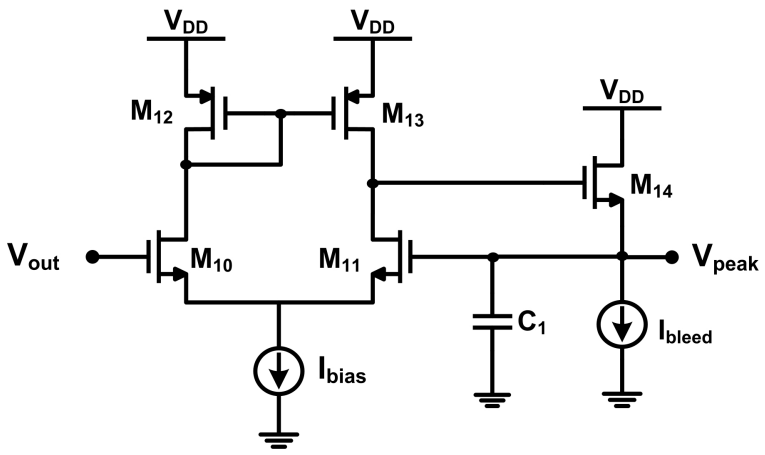



Figure 3.16: Peak Detector schematic.

On the other hand, when $V_{peak}$ surpasses $V_{out}$, the Opamp output voltage clips at the lower supply voltage (GND), forcing $M_{14}$ to be switched OFF. During this period of time, a bleeding current source of 1 $\mu$A discharges the sampling capacitor at a 0.8 MV/s rate. The bleeding current was dimensioned to provide a fast tracking of amplitude variations, but still keeping a reduced ripple at a 20 MHz oscillation frequency.

The MOS transistor $M_{14}$, in turn, was sized to provide enough current to quickly charge the sampling capacitor and, since $V_{peak}$ is up limited by the $M_{14}$ gate-source voltage ($V_{peak_{max}} = V_{DD} - V_{gs,M14}$), a low $V_{th}$ transistor was used for its implementation.

For the sake of power consumption, the operational amplifier was implemented as a single stage differential pair, with a gain of 25 dB and a bandwidth of 100 MHz.

### Comparator

The comparator, in turn, was implemented as a simple two-stage operational amplifier (Figure 3.17). However, considering the design specificities, two important characteristics had to be observed.

In order to set a precise control of the oscillation amplitude and yet provide a strong attenuation of the peak detector output ripple, the operational amplifier was designed to present a reasonably large gain combined with a very limited bandwidth. Therefore, to meet both requirements, a regular two-stage Miller-compensated operational amplifier was implemented.

The design of such amplifiers is extensively discussed in literature, and references such as

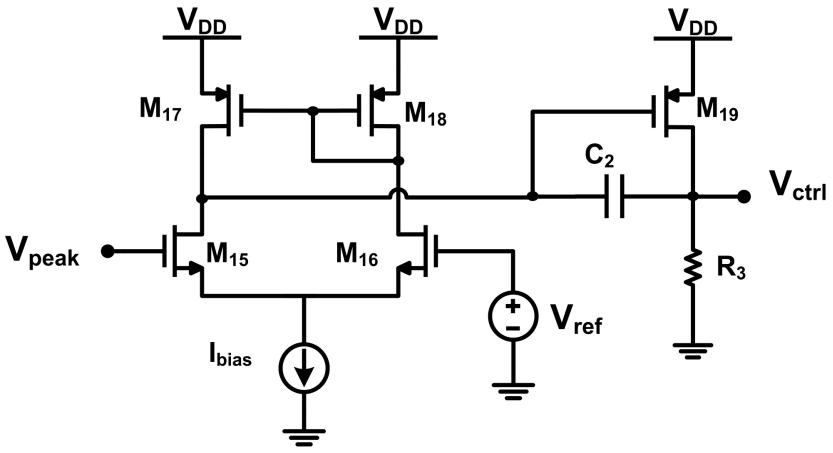



Figure 3.17: Comparator schematic.

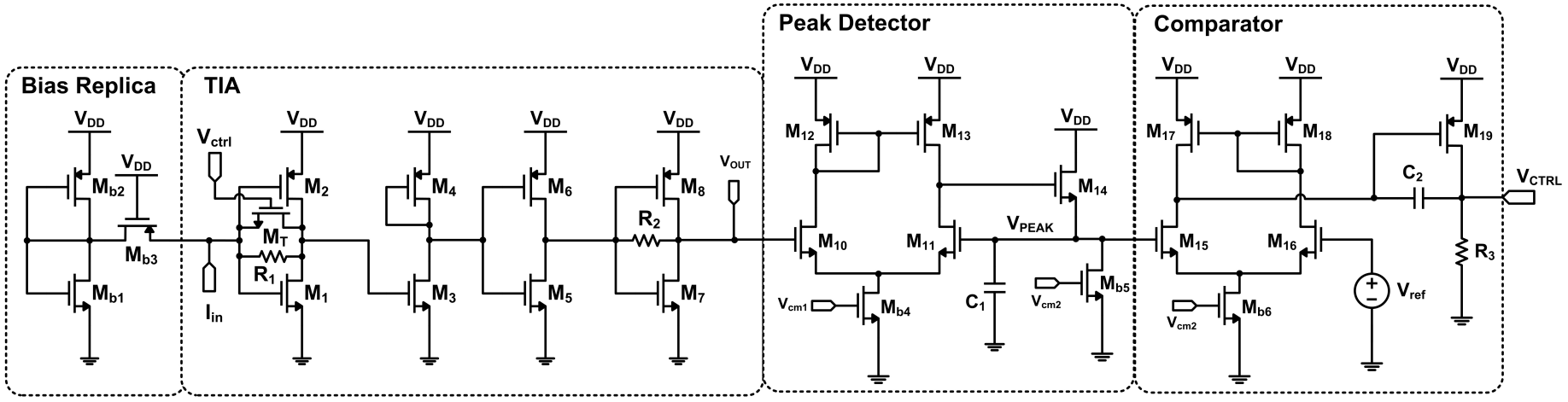
[22][41] were considered during transitor sizing phase.

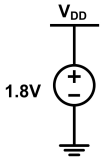
Therefore, the amplifier is expected to achieve a gain of 60 dB, with a phase margin of 85 degrees. By means of a 10 pF Miller capacitance, a very low frequency (200 Hz) dominant pole is expected, so the peak detector output ripple can be filtered out by at least 26 dB attenuation (at 20 MHz).

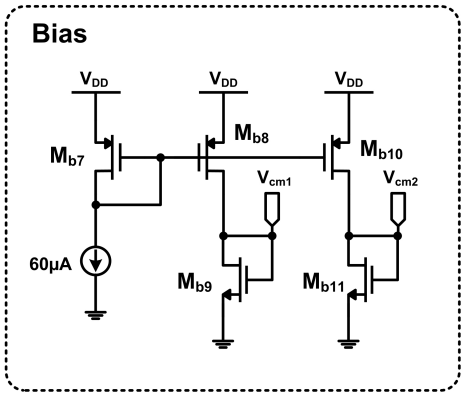
As the peak detector, the comparator was also designed aiming for a reduced power consumption.

## 3.3 Circuit Schematics

Finally, the complete TIA schematics and transistor sizes can be seen in Figure 3.18. The design layout, in turn, is included in Appendix A.




| Bias | Peak Detector | Bias Replica |
|---|---|---|
| $W/L_{b7}$ = 36u/.540u | $C_1$ = 1.2 pF | $W/L_{b1}$ = 30u/.310u |
| $W/L_{b8}$ = 6u/.540u | $W/L_{b4}$ = 20u/.540u | $W/L_{b2}$ = 10u/.310u |
| $W/L_{b9}$ = 20u/.540u | $W/L_{b5}$ = 1u/.540u | $W/L_{b3}$ = 2u/2u |
| $W/L_{b10}$ = 6u/.540u | $W/L_{10}$ = 20u/.180u | |
| $W/L_{b11}$ = 10u/.540u | $W/L_{11}$ = 20u/.180u | |
| | $W/L_{12}$ = 5u/.180u | |
| **Variable-gain Stage** | $W/L_{13}$ = 5u/.180u | |
| $R_1$ = 20 kΩ | $W/L_{14}$ = 4u/1u | |
| $R_2$ = 5 kΩ | | |
| $W/L_T$ = 18u/3u | **Comparator** | |
| $W/L_1$ = 32u/.310u | $C_2$ = 10 pF | |
| $W/L_2$ = 96u/.310u | $R_3$ = 15 kΩ | |
| $W/L_3$ = 10u/.310u | $W/L_{b6}$ = 2u/.540u | |
| $W/L_4$ = 30u/.310u | $W/L_{15}$ = 6u/2u | |
| $W/L_5$ = 32u/.310u | $W/L_{16}$ = 6u/2u | |
| $W/L_6$ = 96u/.310u | $W/L_{17}$ = 2u/.540u | |
| $W/L_7$ = 32u/.310u | $W/L_{18}$ = 2u/.540u | |
| $W/L_8$ = 96u/.310u | $W/L_{19}$ = 60u/.540u | |

Figure 3.18: Complete TIA schematics and device dimensions

Chapter 4

# Results and Discussion

This chapter has the intent to provide a complete performance assessment of the designed transimpedance amplifier. Thereby, a complete set of simulations were held, covering AC, Transient and DC analysis.

Otherwise mentioned, a 500 fF value was considered as a typical interconnection parasitic capacitance ($C_{par}$), and every internal node was loaded with a 50 fF capacitor to account the worst layout parasitics.

At the end, the obtained key performance parameters are compared with the specification, and a results summary is provided by Table 4.1.

## 4.1 TIA Analysis

### 4.1.1 AC Analysis

Figure 4.1 shows the applied test-bench to determine the maximum gain and phase shift for the designed transimpedance amplifier. The simulation results, in turn, can be seen in Figure 4.2.

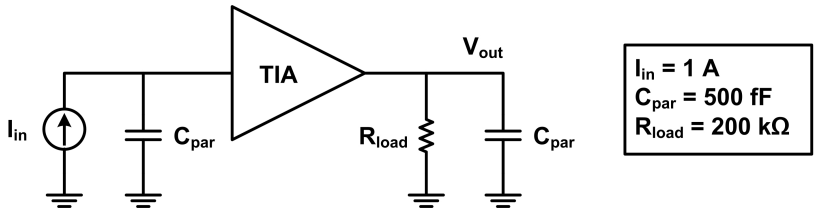



Figure 4.1: TIA AC Analysis test-bench.

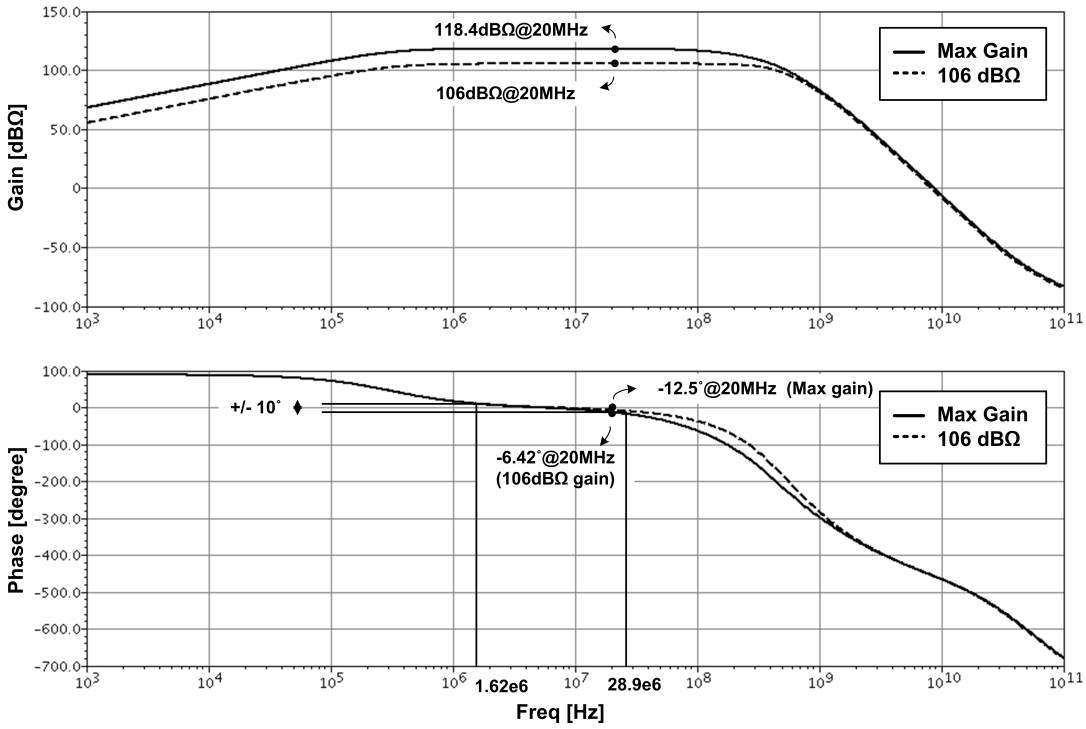



Figure 4.2: Transimpedance Gain and Phase versus Frequency. The dashed line represents the lowered gain condition (106 dBΩ).

As observed, the amplifier presents a maximum transimpedance gain of 118.4 dBΩ, with a resultant -3 dB bandwidth of 140 MHz. The gain parameter is significantly larger than the required by specification, and makes the amplifier suitable to sustain oscillation of resonators with motional resistances up to 800 kΩ.

At maximum gain, the observed phase shift of -12.57 degrees around 20 MHz is above the specified ($<$ 10 degrees). However, if the gain is reduced to the minimum required by specification (106 dBΩ), the phase shift at 20 MHz drops to -6.4 degrees only.

Also shown in Figure 4.2, a wide range of resonant frequencies are accommodated by the amplifier, fitting the 10 degree maximum phase shift within oscillation frequencies from 1.62 to 28.9 MHz.

### 4.1.2 Gain Tunability

As already mentioned, the amplifier gain can be tuned by the adjustment of a control voltage. Shown in Figure 4.3, the employed test-bench provides the means to asses the amplifier gain

tunability, with the control voltage varying within the supply limits, from 0 to 1.8 volts.

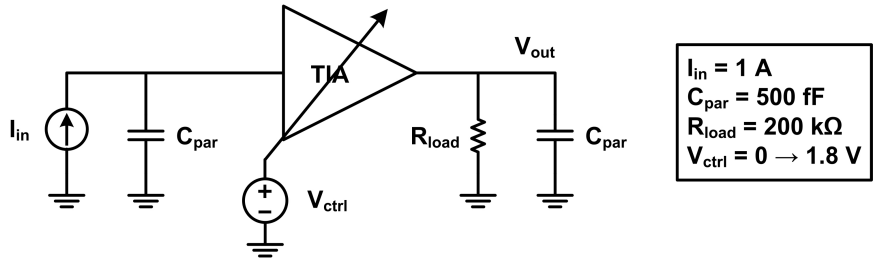



Figure 4.3: TIA Gain and Bandwidth versus $V_{ctrl}$ test-bench.

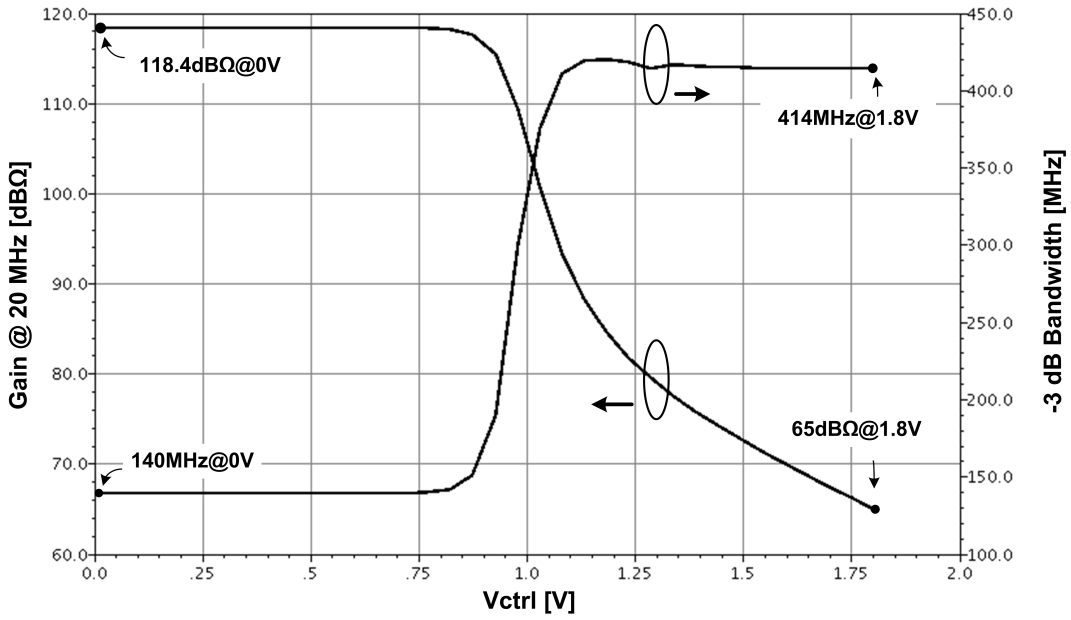



Figure 4.4: TIA Gain and Bandwidth versus Control Voltage ($V_{ctrl}$). As expected, as the gain decreases with $V_{ctrl}$, the bandwidth is augmented.

Seen in Figure 4.4, through the variation of the control voltage ($V_{ctrl}$), the amplifier's transimpedance gain can be adjusted within the maximum and minimum values of 118.4 and 65 dBΩ, respectively. As a result, the designed transimpedance amplifier provides a wide tunning range of 53 dB, making it suitable for resonators with motional resistance ranging from 1.8 to 830 kΩ.

If a minimum gain of 3 (three) is kept to ensure oscillation build-up, the upper limit drops to one third, corresponding to a still large tuning range of 43dB, approximately.

Further noted in Figure 4.4, the circuit bandwidth is also modified with the control voltage variation. This behavior was already expected, since the negative feedback applied in the first stage shifts the dominant input pole to higher frequencies, as the gain is decreased by the action of $V_{ctrl}$. Considering the phase shift limit of 10 degrees, as the bandwidth augments (from 140 to 414 MHz), so does the maximum accommodated oscillation frequency.

Therefore, as seen in Figure 4.5, the transimpedance amplifier can suit resonant frequencies from 16.4 to 39.3 MHz, corresponding to the maximum and minimum gain conditions, respectively.

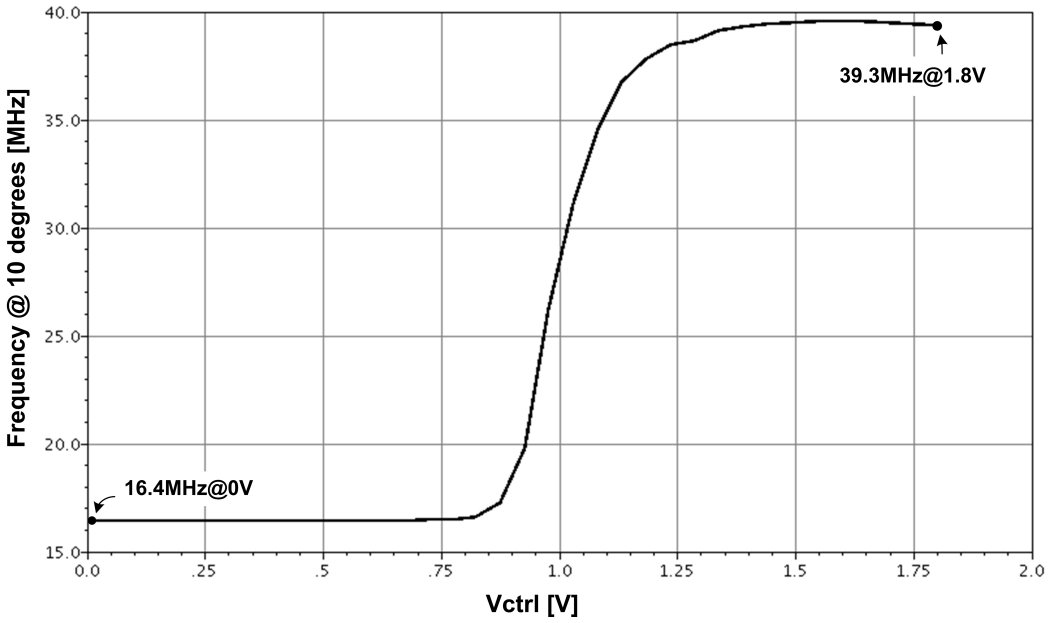



Figure 4.5: Maximum resonant frequency accommodated by the transimpedance amplifier considering the 10 degree phase shift limit.

### 4.1.3 Input and Output Resistance

As mentioned before, due to their impact on both system bandwidth and resonator Quality Factor, the input and output resistances should be kept below a minimum value required by specification (500 Ω). Therefore, with the respective calculations involved (Figure 4.6), the frequency response of such parameters was evaluated, and the results can seen in Figure 4.7.

As noted, for frequencies as high as 20 MHz, the equivalent resistance seen at both input and output nodes are below 1 kΩ.

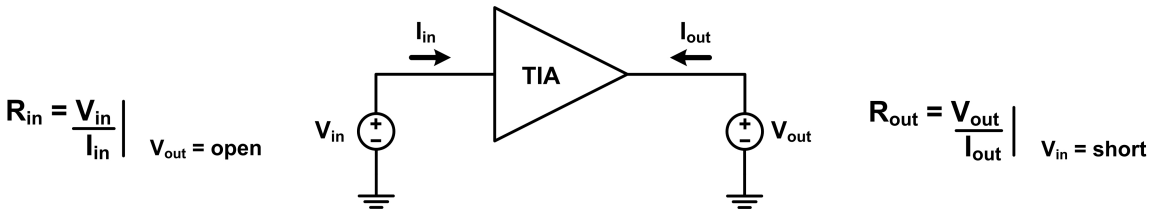



Figure 4.6: TIA Input and Output Resistances versus Frequency test-bench.

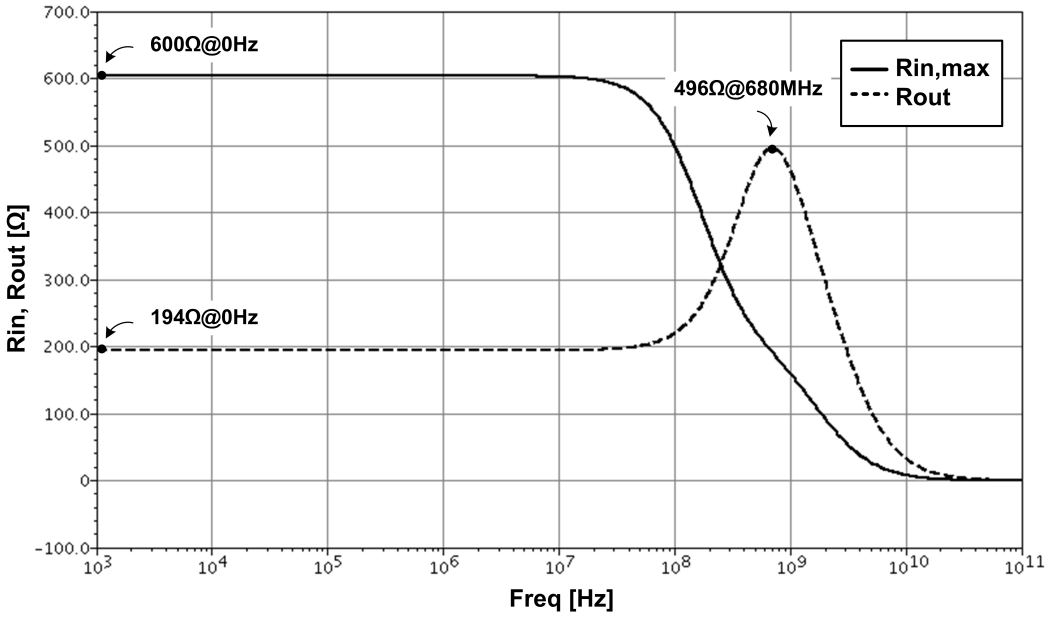



Figure 4.7: TIA Input and Output Resistances versus Frequency. At maximum gain $R_{in}$ does not meet the specification.

Even though apparently the observed input resistance $R_{in,max}$ (600 Ω) does not meet the specification requirement of 500 Ω, it is important to mention that this value corresponds to the maximum transimpedance gain condition. As stated in Equation 3.9, both gain and input resistance of a shunt-shunt feedback amplifier are determined by the feedback resistor, in this case represented by $R_{var}$. As a result, by diminishing the gain, the input resistance decreases as well. This statement can be visualized in Figure 4.8, which gives the amplifier input resistance as a function of the control voltage $V_{ctrl}$ (and gain, consequently).

If the minimum gain required by specification is again considered, it can be seen that the maximum input resistance parameter is met, with a reduced value of 315 Ω.

The output resistance, in turn, first increases as the loop gain is diminished by circuit

parasitics, falling again after additional poles become dominant. Nevertheless, the maximum achieved value of 496 Ω is still in agreement with the specification.

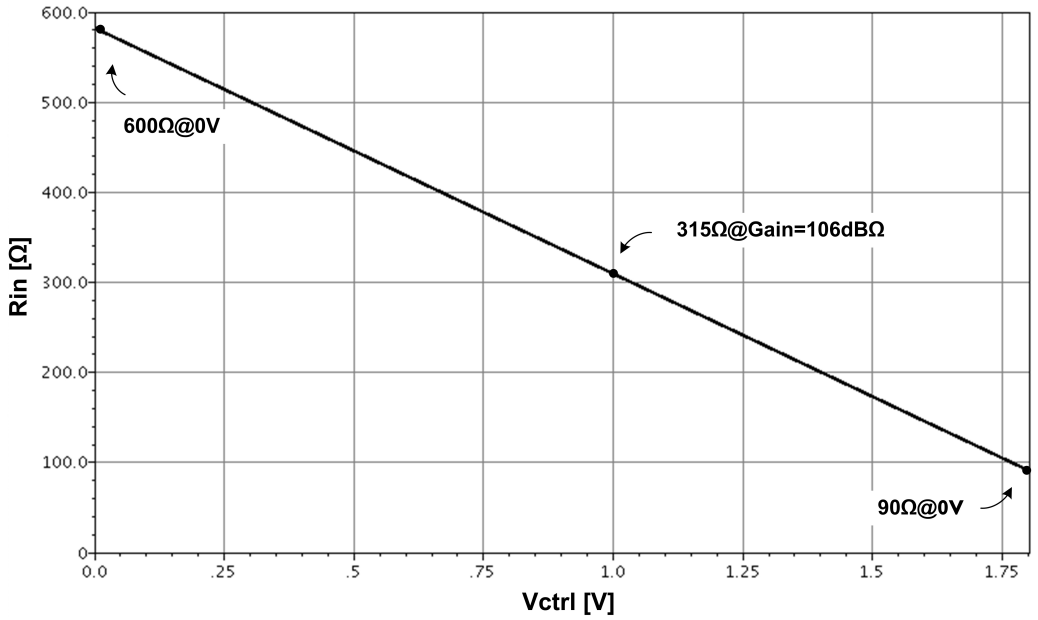



Figure 4.8: TIA Input Resistances versus $V_{ctrl}$. Since the Input Resistance is proportional to the TIA transimpedance gain, as the gain decreases, $R_{in}$ decreases as well.

### 4.1.4 Cpar and Cdec

The system dependency on both decoupling and interconnection parasitic capacitances was evaluated through the test-bench seen in Figure 4.9. Both components impact on the system frequency response, but while $C_{dec}$ is considered as a design parameter and hence can be optimized, the interconnection parasitic capacitance $C_{par}$ is intrinsic to the MEMS resonator and cannot be changed.

First considering the decoupling capacitor, both gain and phase dependencies can be seen in Figure 4.10.

As expected, larger values of $C_{dec}$ leads to a larger gain, but also a bandwidth decrease in same proportion. Moreover, it can be seen that the chosen decoupling capacitance value of 2 pF represents a good trade-off in terms of gain and layout area consumption.

In turn, to check the system sensitivity to the interconnection parasitic capacitance, both gain and phase parameters were observed as $C_{par}$ varies from 0 to 2 pF (Figure 4.11).

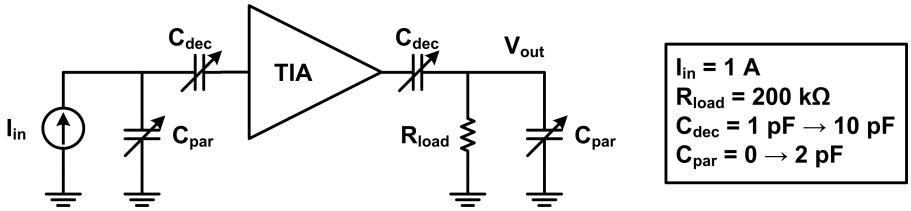



Figure 4.9: TIA Gain and Phase versus $C_{dec}$ test-bench.

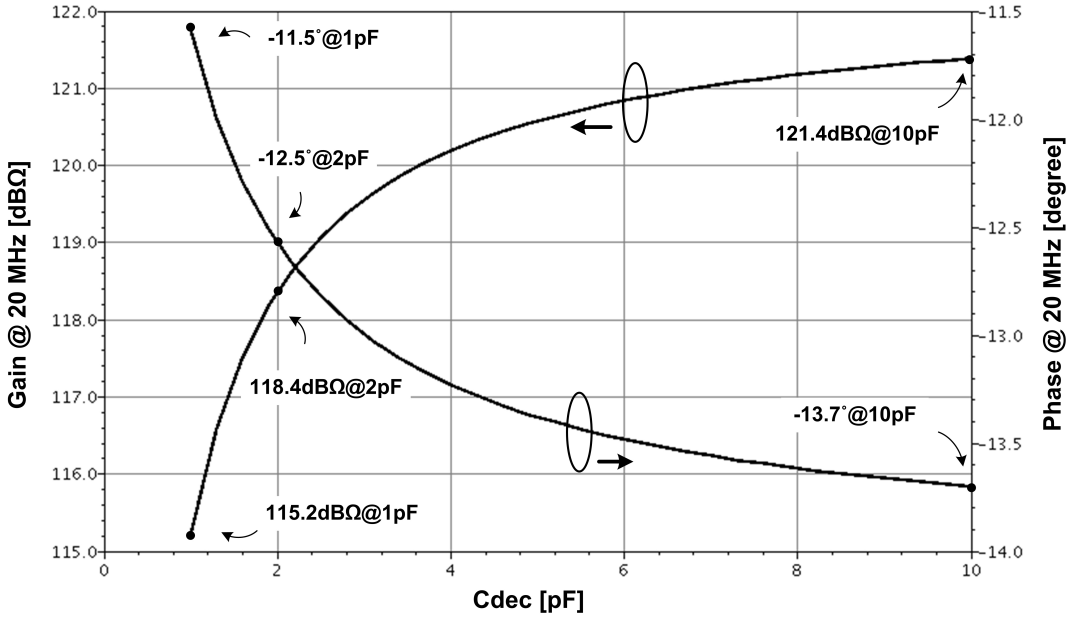



Figure 4.10: TIA Gain and Phase versus $C_{dec}$. The chosen decoupling capacitance value of 2 pF represents a good trade-off in gain/phase shift and layout area.

It can be noted that the parasitic capacitance $C_{par}$ impacts on the system performance by lowering both transimpedance gain and bandwidth, and therefore should be minimized. However, this capacitance is intrinsic to the MEMS resonator and, as such, it does not represent a design parameter.

### 4.1.5 Input-referred Noise Current

As one of the most important parameters to be assessed, the input-referred noise current has a strong influence on the oscillator phase noise (Equation 2.4).

Applying the same test-bench shown in Figure 4.3, the correspondent current noises were evaluated for three different gain conditions.

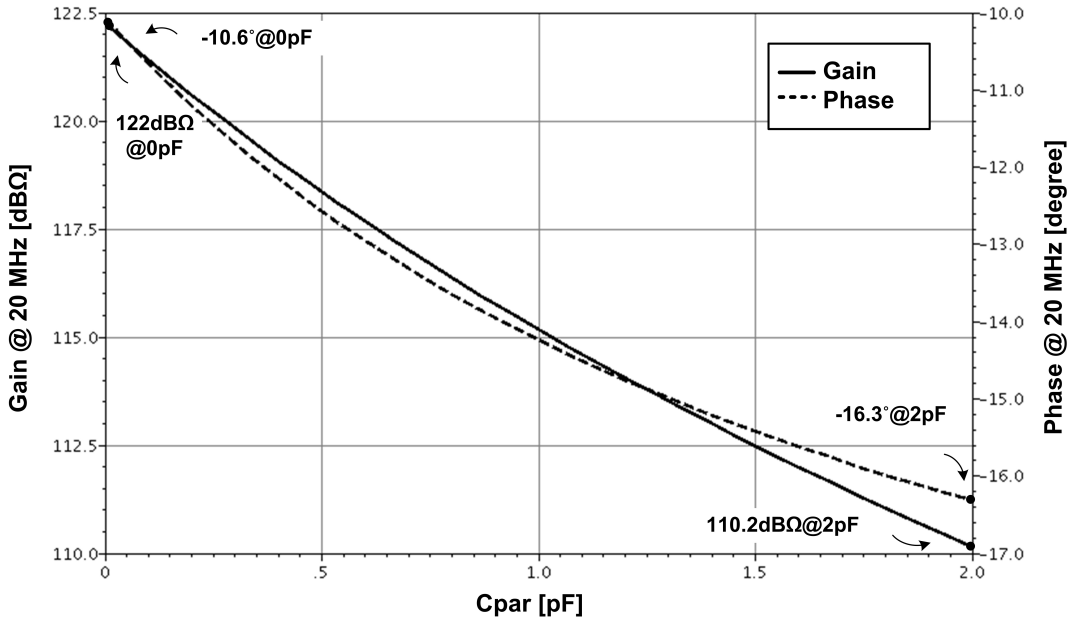



Figure 4.11: TIA Gain and Phase versus $C_{par}$. As noted, $C_{par}$ has a significant impact on the system frequency response. Typical and worst-case values are expected to be 500 fF and 1 pF, respectively.

The overall noise performance of any cascade of amplifying stages is highly dependent on the earlier stages. This conclusion comes from the statement that all subsequent stage's noise contributions are attenuated by the former stage's gain, as seen in Equation 3.20. Therefore, as observed in Figure 4.12, higher input-referred noise levels are obtained for lower gain conditions.

Nevertheless, even though at minimum gain a considerable input-referred noise current of 219 pA/$\sqrt{}$Hz was achieved, from close-mid to maximum gain the TIA meets the specification parameter, with a minimum input noise current of 2.51 pA/$\sqrt{}$Hz.

### 4.1.6 Corner Analysis

It is known that fabrication processes are not completely uniform and, if both temperature and supply voltage variations are also accounted, a wide combination of operation conditions can be generated. Named 'corners', they represent different worst-case conditions, in which the designed amplifier should be still functional.

Also using the test-bench shown in Figure 4.3, 45 PVT combinations were simulated, covering most of the process corners, with +/- 10% supply voltage variation and temperature ranging

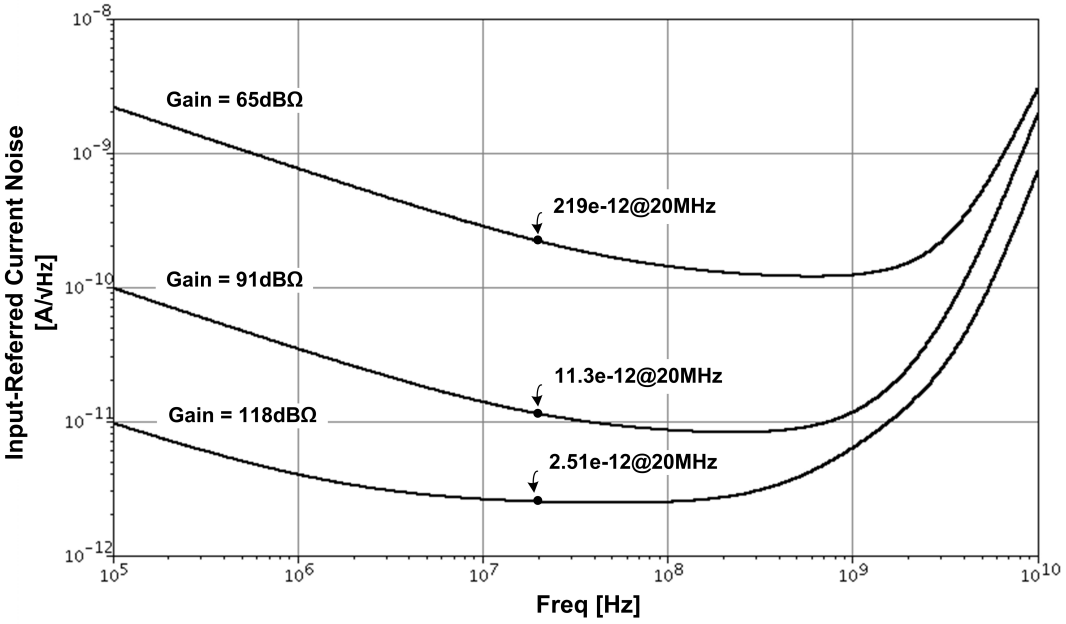



Figure 4.12: TIA Input-referred Noise Current versus Frequency for Maximum (118 dBΩ), Minimum (65 dBΩ) and Middle (91 dBΩ) gain conditions.

from -40° to 125° C. The results can be seen in Figure 4.13 and 4.14.

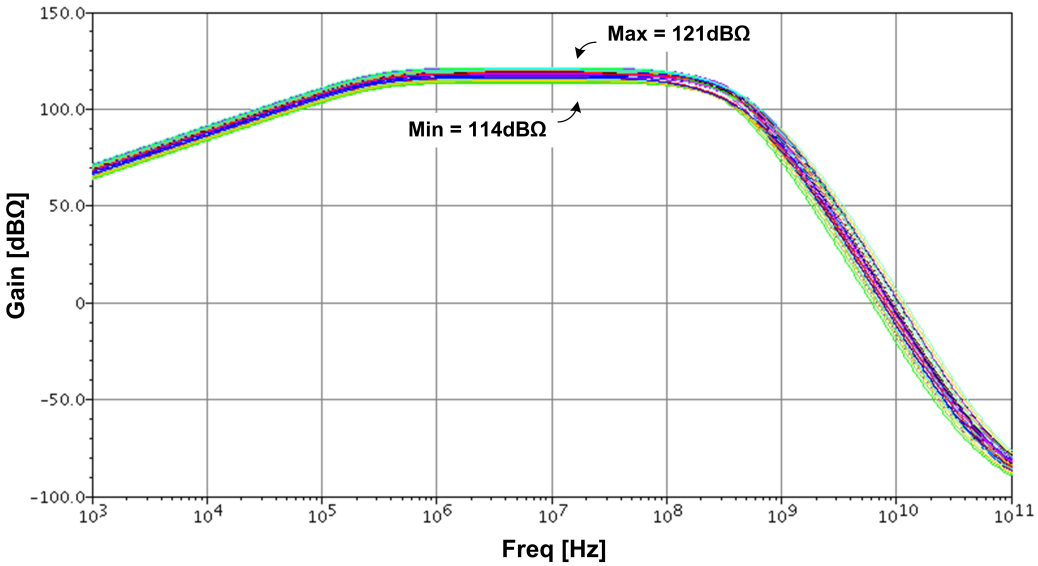



Figure 4.13: TIA Gain Corner Simulations. For every simulated corner the gain specification parameter was met.

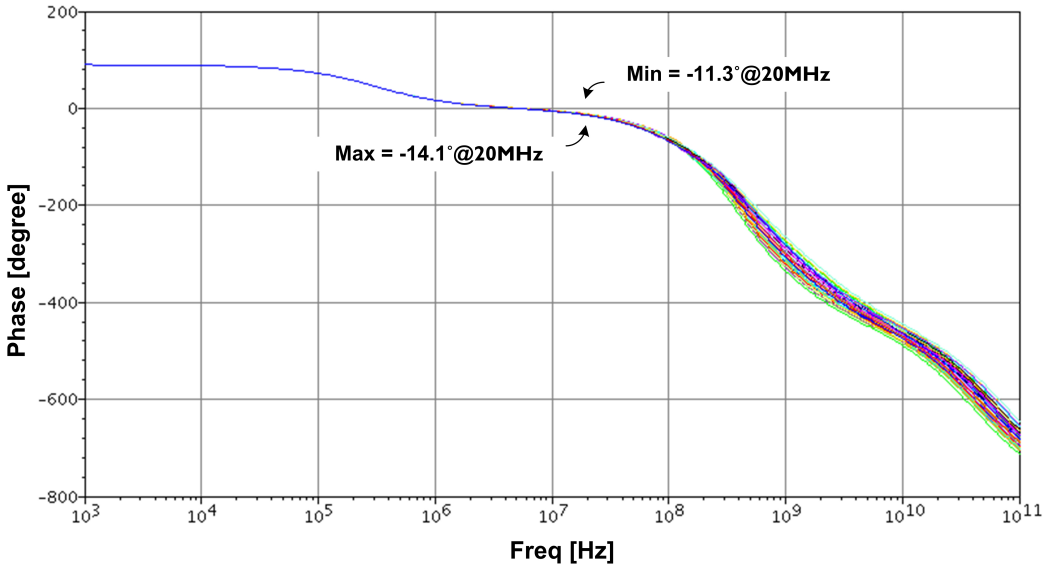



Figure 4.14: TIA Phase Corner Simulations. Only a small deviation of 2.8 degrees are observed between all the simulated corners.

Specially when considering the application of large gain amplifiers, the corner simulations may represent too severe operation conditions. However, as noted in Figure 4.13, the TIA was kept operational in every corner simulation, mainly due to the application of the replica biasing method. Despite the somewhat large gain variation of 7 dBΩ, in the worst-case the TIA still meets the minimum gain required.

Furthermore, as seen in Figure 4.14, the design is also very robust considering the phase parameter, which varies within a very little range (from -11.3 to -14.1 degrees).

### 4.1.7 Transient Analysis

In order to observe a 1 $V_{peak-peak}$ output signal at maximum gain condition, a 20 MHz sinusoidal input current of 1.2 $\mu$A amplitude was applied (Figure 4.15).

As seen in Figure 4.16, it is very difficult to note any distortion in the output signal, which is also confirmed once its spectral content is verified. For the same 1 $V_{peak-peak}$ output signal, a Total Harmonic Distortion (THD) of only 2% is obtained, which can be considered as another important feature of the employed topology.

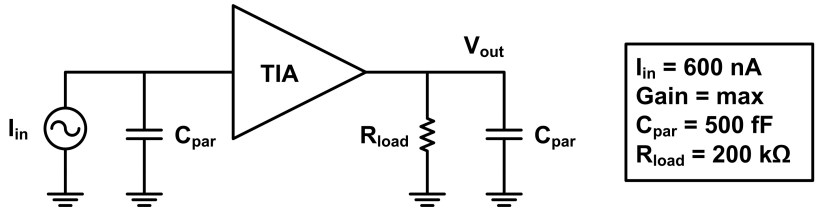



Figure 4.15: TIA Transient Analysis test-bench.

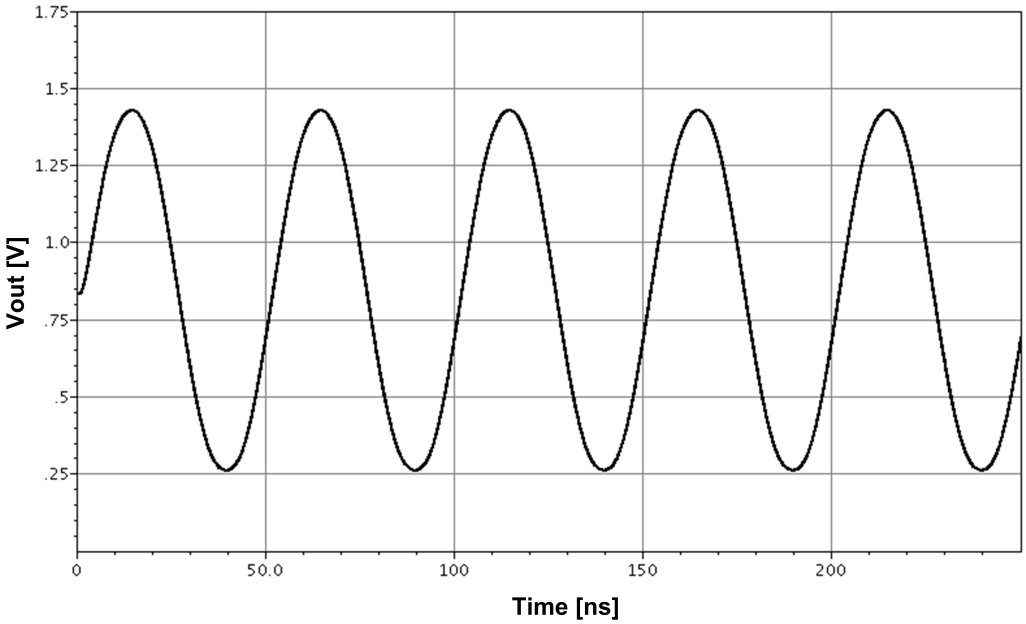



Figure 4.16: TIA Transient response. As observed, the topology provides a low output harmonic distortion.

## 4.2 AGC Analysis

### 4.2.1 Peak Detector

To asses the transient behavior of the designed peak detector, a 200 kHz signal was modulated in amplitude (AM) with a 20 MHz carrier (Figure 4.17). For a complete evaluation, the comparator was included to account its loading effect at the output, and the simulation results can be seen in Figure 4.18.

The bold line represents the peak detector output signal, which is refreshed every time $V_{in}$ surpasses $V_{peak}$ (in detail). Also noted, once the oscillation amplitude approaches the supply voltage, the peak detector presents a small error of approximately 100 mV, which is believed

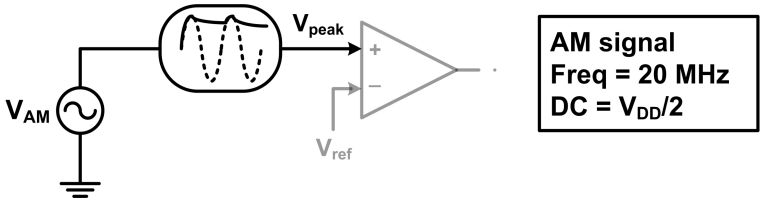



Figure 4.17: Peak Detector Transient Analysis test-bench.

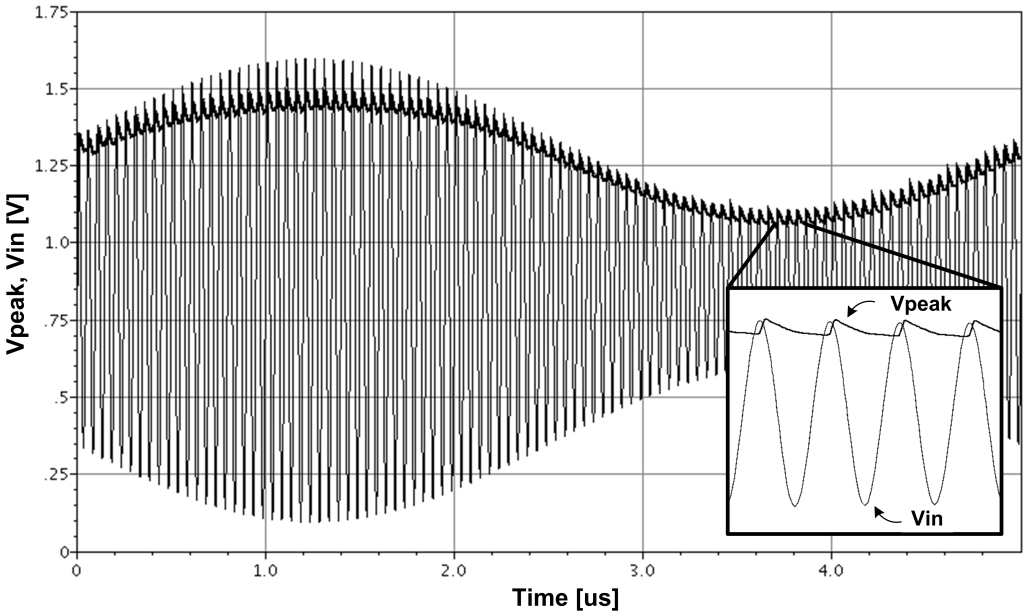



Figure 4.18: Peak Detector Transient response. In detail, the charge and discharge of the sampling capacitance.

to be caused by the voltage headroom limitation imposed by $M_{14}$ gate-source voltage (Figure 3.16).

It can also be seen that the designed bleeding current provides the means to quickly track oscillation amplitude variations, represented in this case by the 200 kHz modulated signal.

### 4.2.2 Comparator

Also taking part of the Automatic Gain Control circuitry, the comparator has the relevant role of generating the control voltage, in a way that the oscillation amplitude is approximated to its reference $V_{ref}$.

For the sake of precision and stability, the comparator must provide a large gain at low

frequencies, combined with a also large attenuation at the oscillation frequency (to filter out the peak detector output ripple). Therefore, through the application of the test-bench seen in Figure 4.19, the comparator frequency response was analyzed.

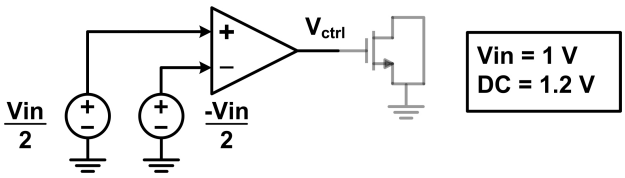



Figure 4.19: Comparator AC Analysis test-bench.

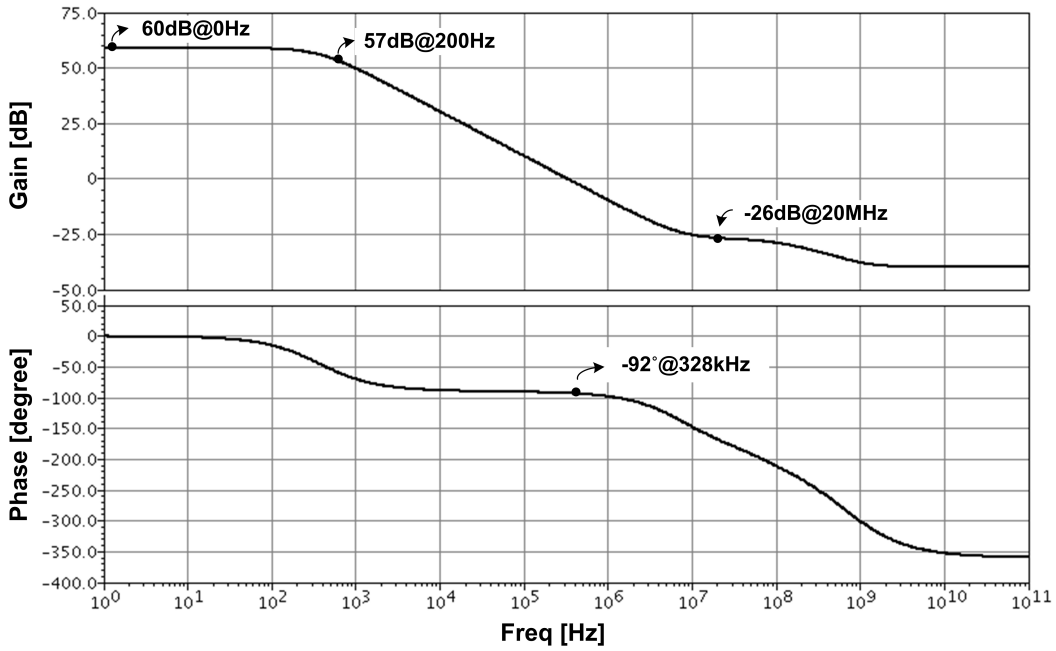



Figure 4.20: Comparator Frequency response. A lowered dominant pole guarantees -26 dB attenuation at 20 MHz.

Seen in Figure 4.20, as demanded the designed comparator presents a large DC gain of 60 dB, with a phase margin of 88 degrees. Equally important, with a low frequency dominant pole at 200 Hz, approximately -26 dB of attenuation is observed at 20 MHz. The attenuation could have been made more aggressive with the addition of more poles, or the further multiplication of the Miller capacitance by increasing the gain of the second stage. However, this improvement was left for future consideration.

### 4.2.3 Transient Analysis

By closing the loop with the Variable-gain Amplifier, it was possible to verify the Automatic Gain Control functionality.

A sinusoidal input current of 4 $\mu$A amplitude was applied, and a reference voltage ($V_{ref}$) of 1.3 V was set (Figure 4.21). The resultant transient response is shown in Figure 4.22.

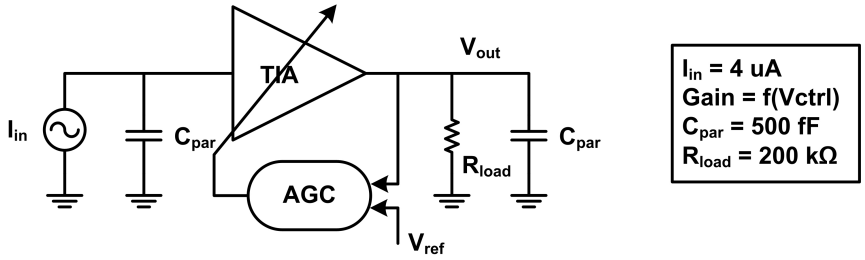



Figure 4.21: TIA + AGC Transient Analysis test-bench.

Due to the comparator low cutoff frequency, the control voltage presents a large time constant. However, after only 8 $\mu$s the gain adjustment is noticed, and the output amplitude stabilizes at 1 $V_{peak-peak}$.

A small error of 3.8% is observed between the output peak value and the set reference voltage ($V_{ref}$), which is believed to be mainly caused by the peak detector measurement imprecisions. Nonetheless, the gain control loop is stable, and after achieving steady-state operation, the control voltage presents a maximum ripple amplitude of only 2 mV.

## 4.3 Example Oscillator Analysis

As already mentioned, the design of the MEMS resonator was beyond the scope of the reported design. However, to obtain a good performance evaluation of the TIA, the system level simulation of a complete oscillator would be necessary. Therefore, to provide the resonator's parameters, a MEMS-based oscillator was chosen from literature (10-MHz CC-beam resonator, described in [8]). As a result, it was possible to check if sustainable oscillation could be achieved, and the resultant phase noise performance.

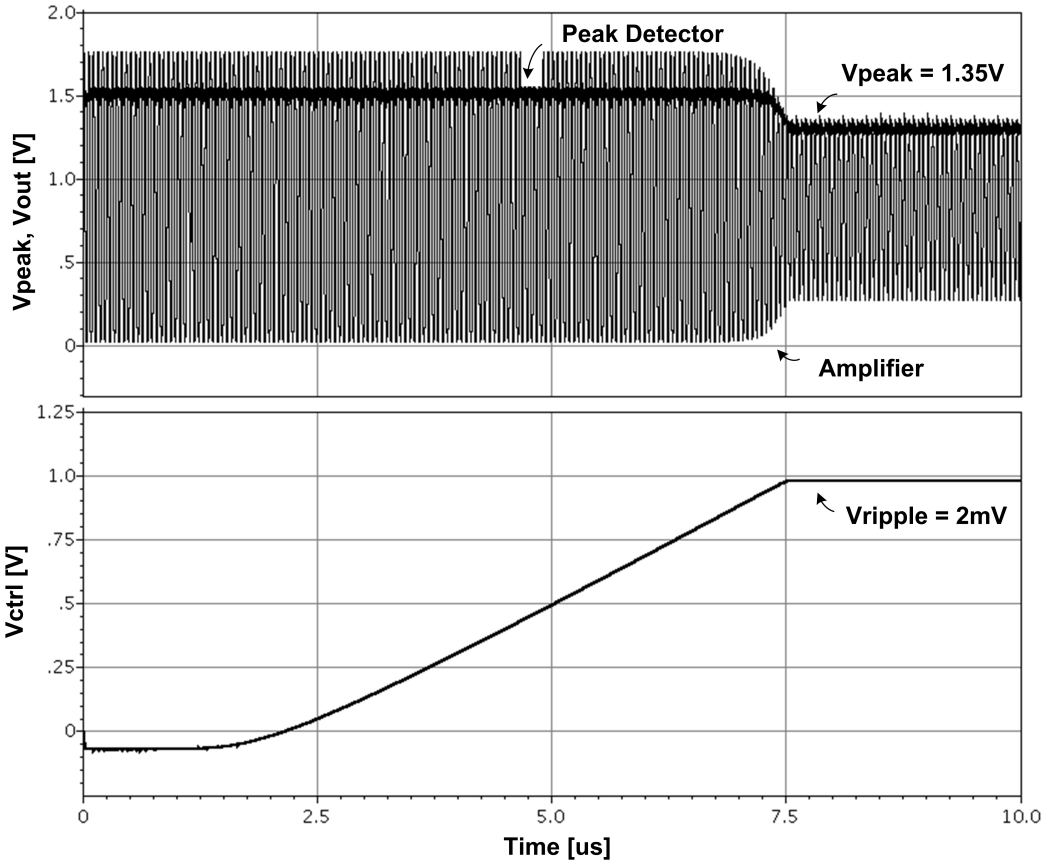



Figure 4.22: TIA + AGC Transient response. After 8 $\mu$s the output amplitude is stabilized with a peak value set by $V_{ref}$.

### 4.3.1 Transient and Phase Noise Analysis

Seen in Figure 4.23, the applied test-bench represents the simulated oscillator, with the designed TIA in closed-loop with the reference resonator.

After a 10 ns simulation period, a short disturbance is applied at the sustaining amplifier output node, which is sufficient to drive the whole system into oscillation (seen in Figure 4.24).

After the oscillation build-up the AGC control action can be noted, and in less than 8 $\mu$s the system achieves steady-state with sustained oscillation.

For the chosen resonator, the obtained Phase Noise parameters at 1 kHz, 10 kHz and 100 kHz offset frequencies was respectively -91, -100 and -109 dBc/Hz.

In comparison with the reference, it represents a relevant performance improvement at 1 kHz offset (-82 dBc/Hz), but for the remainder offset frequencies, the achievements are below

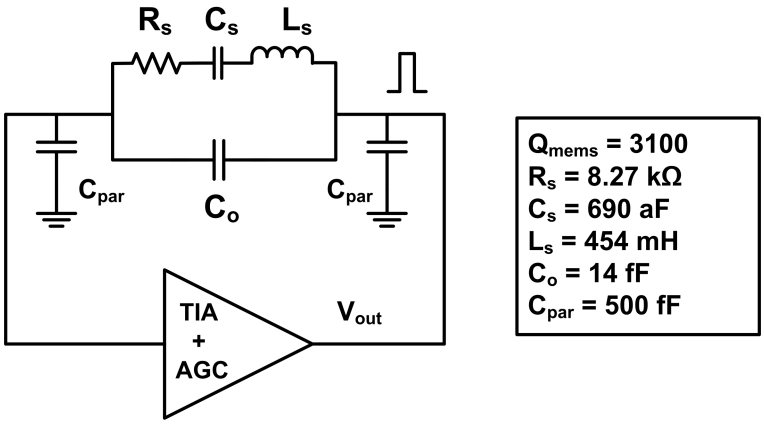



Figure 4.23: Example Oscillator Transient and Phase Noise Analysis test-bench.

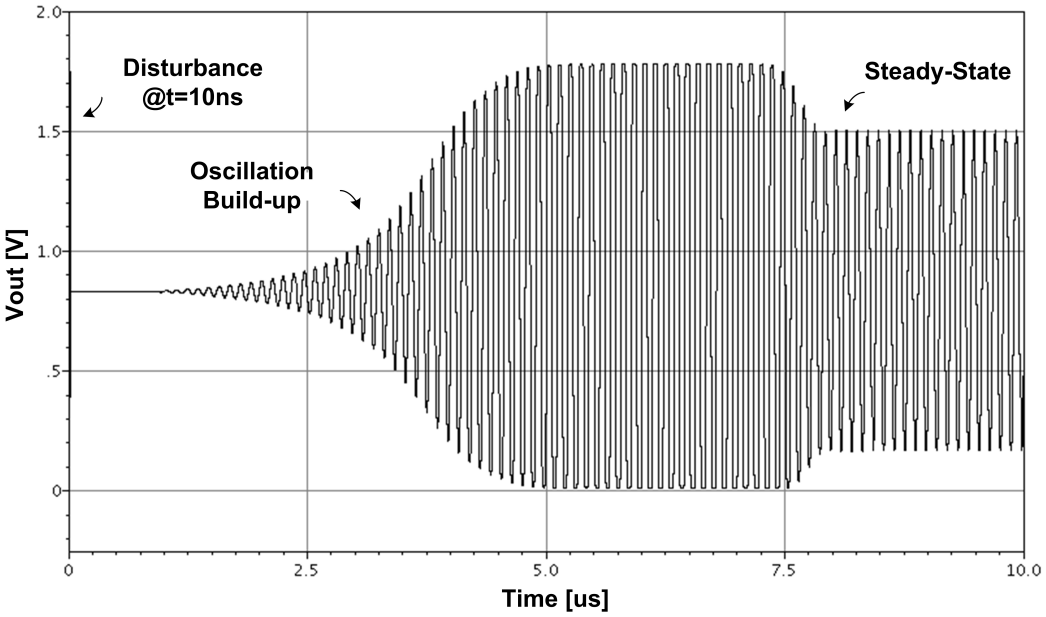



Figure 4.24: Example Oscillator Transient behavior. With a reference resonator, it is possible to observe the complete functionality of the TIA system.

the reported (-110 and -116 dBc/Hz).

However, it is very important to notice that, to overcome the resonator's motional resistance of 8.27 kΩ, the designed TIA is put in its lower gain condition. As already mentioned, in such situation the amplifier presents a significantly higher input-referred noise current, what is believed to be the cause of a increased Phase Noise parameter for higher frequency offsets.

Nevertheless, the obtained Phase Noise results can be considered as very promising, since a

even better TIA noise performance can be expected with higher motional resistances.

## 4.4 Results Summary

A summary of the simulated TIA parameters, as well as similar reported designs, are provided by Table 4.1. With different applications, for a fair comparison between the designs, a widely-accepted Figure of Merit (FoM) [42] provided by Equation 4.1 was employed.

$$FoM = \frac{GBW}{P_{DC}} \tag{4.1}$$

where GBW represents the amplifier's gain-bandwidth product, and $P_{DC}$ is the static power consumption.

Table 4.1: Results Summary.

| | | This work [1] | | | | | |
|---|---|---|---|---|---|---|---|
| Parameter | Spec. | Max | 200 kΩ | [1] | [43] | [26] | Units |
| Gain | > 106 | 118.4 | 106 | 76 | 82 | 155 | dBΩ |
| BW | N.D. | 140 | 333 | 2500 | 2400 | 1.8 | MHz |
| Phase Shift @ 20 MHz | < 10 | -12.5 | -6.4 | N.A. | N.A. | ≫ 10 | degrees |
| $R_{in}$ | < 500 | 600 | 315 | <50 | <50 | N.A. | Ω |
| $R_{out}$ | < 500 | 194 | 194 | 50 | N.A. | N.A. | Ω |
| Input-referred Noise [2] | < 10 | 2.51 | 3.94 | <10 | 19 | 0.065 | $pA/\sqrt{Hz}$ |
| Gain Tunability | N.D. | 53 | 41 | 12 | 6 | 0 | dB |
| GBW/$P_{DC}$ | N.D. | 38.8 | 22.2 | 2.19 | 1.54 | 231 | THzΩ/mW |
| Power ($P_{DC}$) | < 1 mW | 3 | 3 | 7.2 | 19.5 | 0.436 | mW |
| CMOS Process | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | μm |

Even though the designed TIA presents a significantly lower bandwidth in comparison to [1] and [43], its large transimpedance gain, combined with a lowered power consumption, provides a distinguishable performance, translated into a high GBW/$P_{DC}$ value.

In turn, when compared to [26], the TIA does not provide a comparable FoM, but if the gain tunability is considered, this design finds a much wider applicability.

[1] Simulated.

[2] The input-referred noise of references [1], [43] and [26] are respectively given at the frequencies of (0.1 - 1 GHz), 1 GHz and 100 KHz.

Finally, as observed in Table 4.1, at maximum gain condition the TIA nearly attends the specification requirements, which are completely met once the transimpedance gain is reduced to the minimum required (106 dBΩ).

Chapter 5

# Conclusion

The design here reported consists of a Variable-gain Transimpedance Amplifier, conceived to provide oscillation sustaining for a MEMS-base oscillator.

Due to a small form factor and a high integrability with common CMOS processing, the design of high Quality Factor MEMS resonators have drawn a lot of attention during the past decade. However, to address specific characteristics of such resonators, the correspondent sustaining amplifier should present a quite challenging set of requirements, such as a high Gain-Bandwidth Product, combined with a both low terminal resistances and noise parameter.

After a preliminary literature survey, the shunt-shunt feedback topology was defined as the most suitable in terms of gain and noise performance.

Therefore, by cascading similar inverting amplifiers with shunt-shunt feedback at both input and output stages, it was possible to obtain a high transimpedance gain of 118.4 dBΩ, with a considerably large bandwidth.

Moreover, with a large gain tunability of 53 dB, the obtained transimpedance amplifier is suitable to provide oscillation sustaining for a wide combination of MEMS resonators, with motional resistances varying from 1.8 to 830 kΩ.

Also in terms of frequency, at different gain conditions, the TIA is able to accommodate resonant frequencies from 16.4 to 39.3 MHz, with less than 10 degrees of phase shift, which is another specification requirement.

To increase the bandwidth and not degrade the resonator Quality Factor, the application of shunt-shunt feedback at both input and output stages confers the amplifier an equivalent terminal resistance of less than 600 ohms, even in the worst-case (maximum gain condition).

On top, considering its significant impact on the resultant oscillator phase noise performance, the amplifier was also designed to present a low input-referred noise current parameter. Resulting from the improved noise performance of the shunt-shunt topology, the presented design was able to achieve, at maximum gain, the considerably low value of 2.51 pA/$\sqrt{}$Hz. This statement, however, does not hold for low gain conditions, when the amplifier input-referred noise current increases significantly.

Nevertheless, the designed TIA is believed to be a complete solution for good performance MEMS-based oscillators.

The implementation of an Automatic Gain Control circuitry, together with the Variable-gain Transimpedance Amplifier, further augments the design applicability. Phase noise degradation related to a MEMS reduced Power Handling Capability are hence addressed by the TIA system. Furthermore, by the employment of a Replica Biasing method, for every combination among a wide range of process, supply voltage and temperature corners, the gain specification parameter was met, and very little phase shift variation was observed.

After layout, with pads excluded, the whole amplifier has occupied a minimal area of 0.018 mm$^2$, and the power consumption is expected to be around 3 mW from a 1.8V supply.

Finally, all the above mentioned comprises a very appreciable set of features, and the designed TIA can be considered as a distinct piece of work. More importantly, throughout the whole design, this TIA represented a great opportunity for the Author to learn and deepen his knowledge, vastly contributing to his expertise.

At last, this work was accepted for presentation at the $3^{rd}$ Latin American Symposium on Circuits and Systems (LASCAS 2012), with the submitted paper attached in Appendix B.

## 5.1 Future Works

Once the design is currently being fabricated, future works will include the test chip characterization. Therefore, a whole set of measurements will be performed, with the intention of validating the presented simulations. The design functionality will be first confirmed through open-loop characterization, and if MEMS resonators are not made available, conventional quartz crystals will be employed to assess the closed-loop operation. Furthermore, since the test chip also includes a replica of the whole TIA with every building block isolated, each system component will be individually characterized.

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Appendix A

# Design Layout

The whole TIA system was laid out for fabrication, using the same XFAB 0.18um technology files.

The top-level view of the complete generated layout can be seen in Figure A.1.

As a test chip, the upper entity represents the designed TIA, with the AGC and decoupling capacitors included.

The lower entity, in turn, comprises the same TIA system, but with each building block (Variable-gain Amplifier, Peak Detector and Comparator) separated for individual assessment. It was also included, before layout, an analog multiplexer in order to open the Gain Control Loop, and externally define the transimpedance gain. Additionally, the inclusion of the multiplexer also augments the design observability.

During layout phase, special care was taken with the Variable-gain Amplifier. To assure reduced offset voltages caused by $V_{th}$ variations, each NMOS and PMOS transistor of the amplifier chain was isolated through a individual guard ring.

Moreover, throughout the entire design, every critical transistor from the schematic was divided into a optimal number of unit transistors, so they could be laid out using a common centroid approach. As a result, a better matching is expected to be achieved, aiming for a increased production yield.

At last, the entire transimpedance amplifier, accounting the AGC and bias circuitry, fits a small area of 97 $\mu$m x 190 $\mu$m, or 0.018 mm$^2$ approximately. The building blocks are indicated and can be seen from Figure A.2 to A.4.

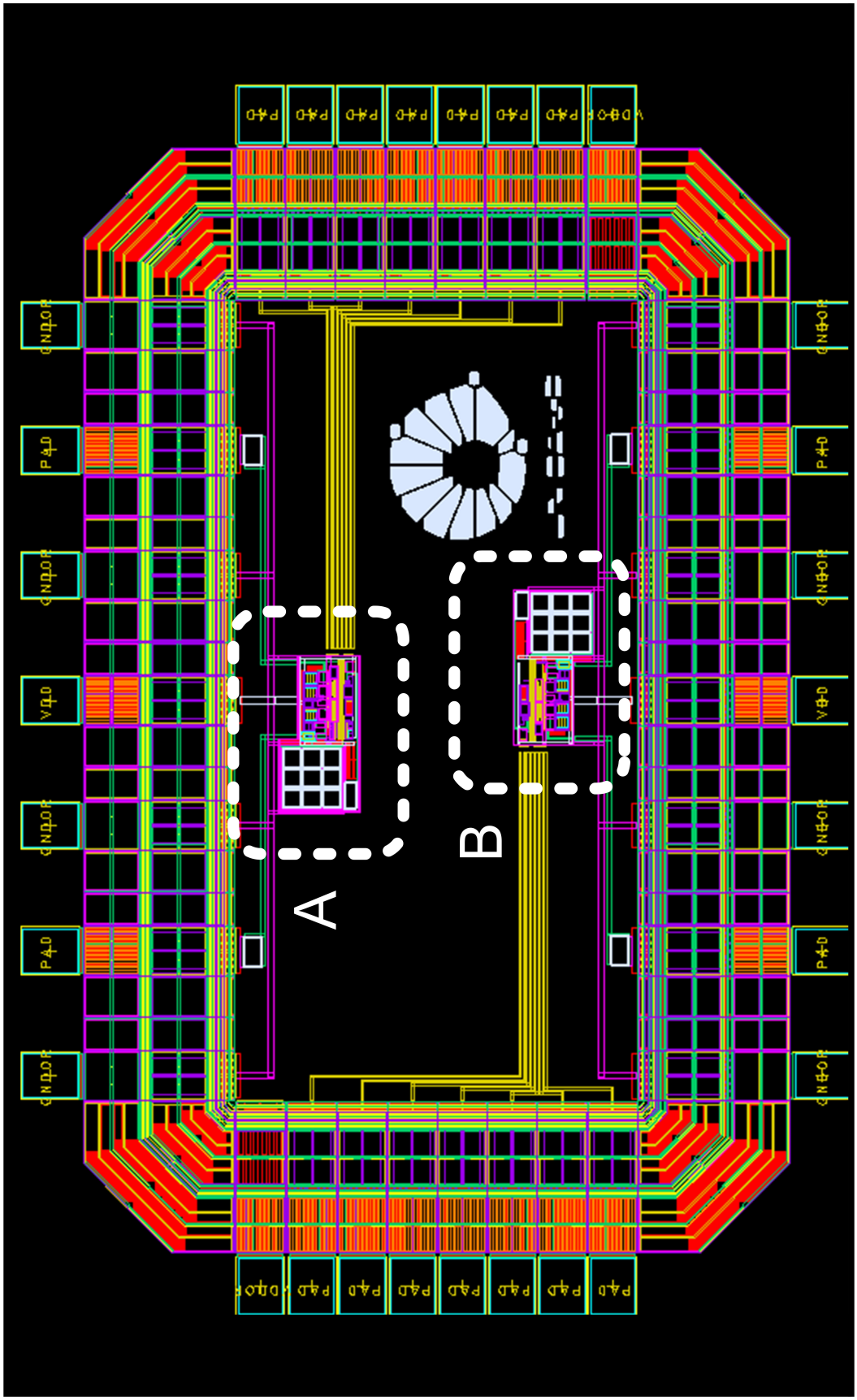


Figure A.1: Complete Test chip layout. A) TIA system with all components interconnected and B) System replica with individualized building blocks.

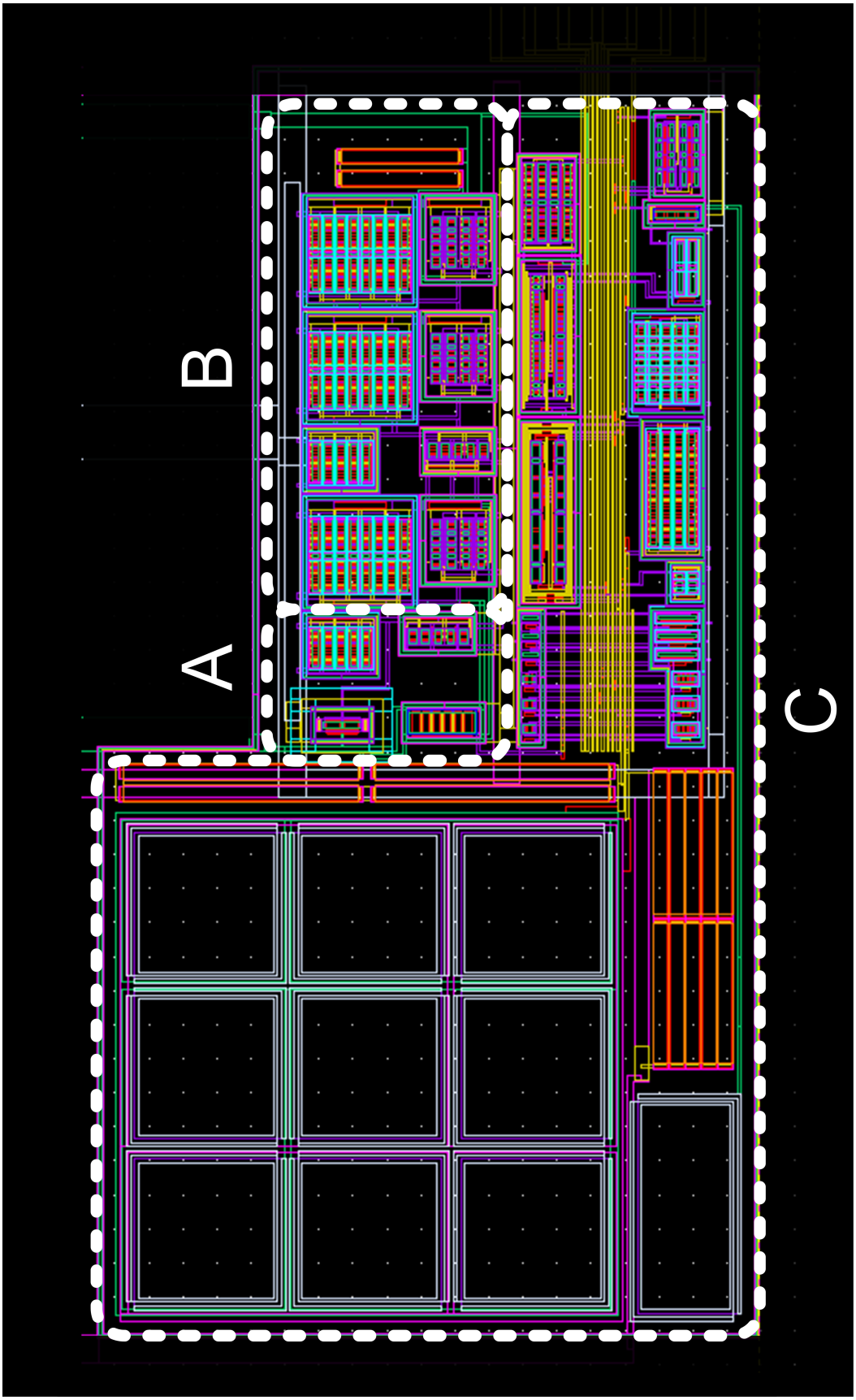


Figure A.2: TIA system layout overview. A) Bias Replica and Rvar; B) Variable-gain Transimpedance Amplifier and C) Automatic Gain Control circuitry.

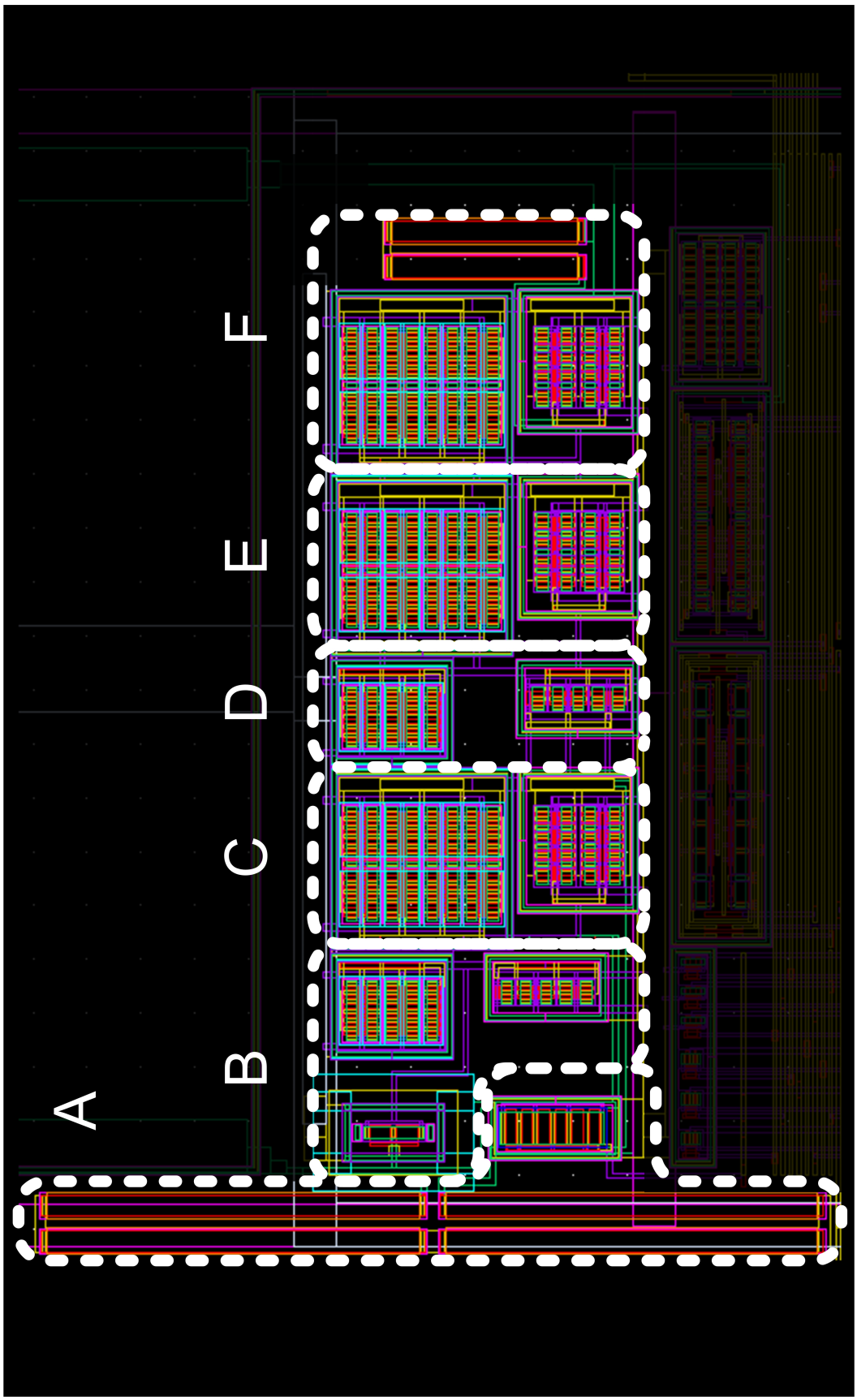


Figure A.3: Variable-gain Transimpedance Amplifier and Bias Replica layout overview. A) Rvar; B) Bias Replica; C) First stage; D) Second stage; E) Third stage and F) Fourth stage.

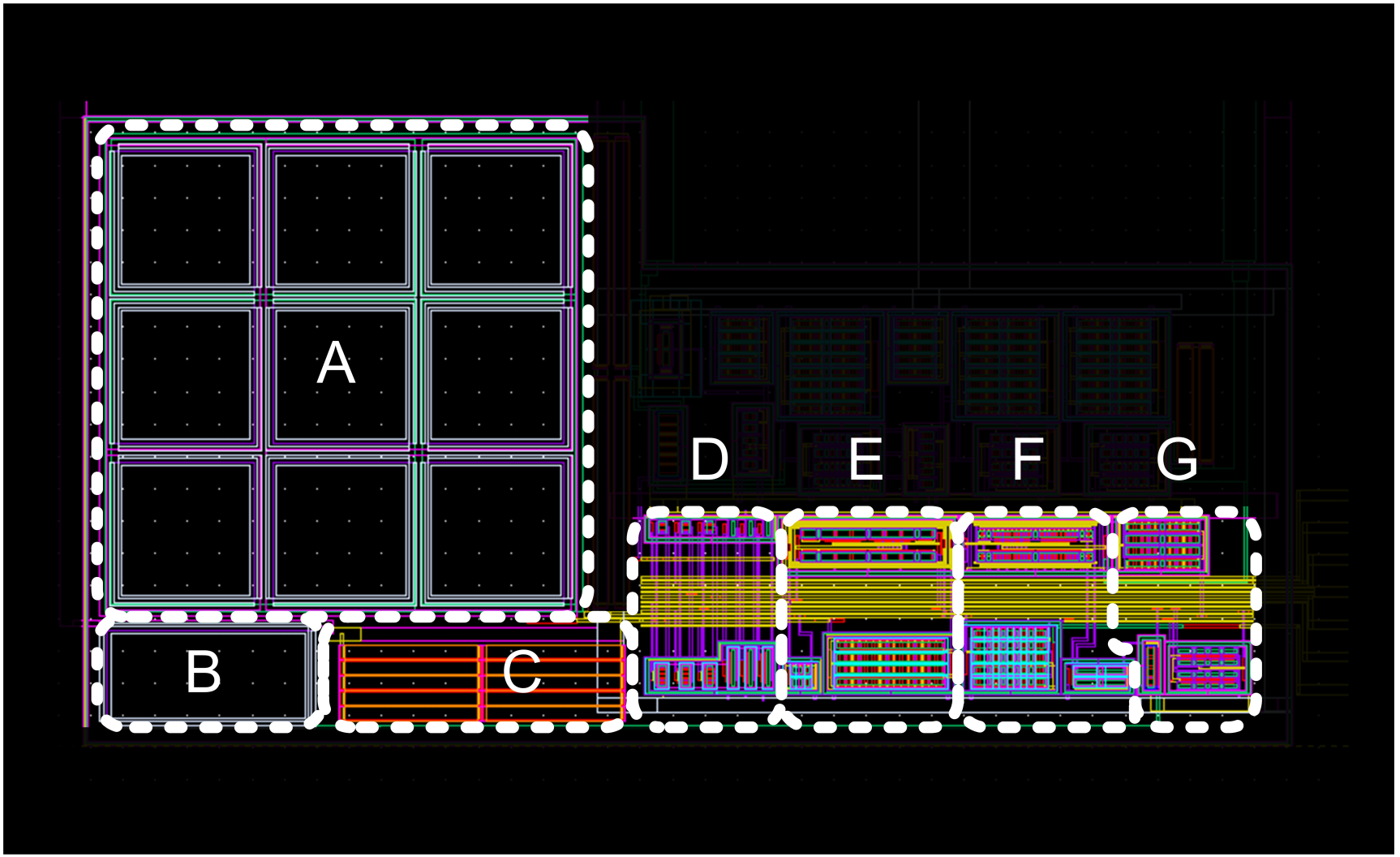


Figure A.4: AGC layout overview. A) Miller capacitance C2; B) Sampling capacitance C1; C) R3; D) Analog Multiplexer; E) Comparator; F) Peak Detector and G) AGC Bias.

Appendix B

# Paper LASCAS 2012

Paper submitted and accepted for presentation at the $3^{rd}$ Latin American Symposium on Circuits and Systems (LASCAS 2012), held in Playa del Carmen, Mexico, from February $29^{th}$ to March $2^{nd}$, 2012.

# A 53dBΩ Tuning Range 5.66pA/$\sqrt{Hz}$ 3.2mW Variable Gain Transimpedance Amplifier for MEMS-Based Oscillators

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***Abstract*— A variable gain Transimpedance Amplifier (TIA) is presented. Realized in 0.18um technology to provide a sustaining amplifier for Micro-Electro-Mechanical System (MEMS) - based oscillators, the reported design combines wide gain tunability (53dBΩ - from 120Ω to 58kΩ) with reduced input-referred noise (5.66pA/$\sqrt{Hz}$ at maximum gain). The general topology consists of four inverter stages cascaded, with shunt-shunt feedback to decrease the amplifier's input and output impedances. The overall system also incorporates an Automatic Gain Control (AGC) circuit to limit the impact of the resonator's non-linearities on system's phase noise, and both terminals are capacitively decoupled, so the MEMS resonator can be independently biased.**

## I. Introduction

Oscillator's market represent a big slice of the electronics industry and, as in any other, the search for smaller, better performance and yet lower power devices is strongly present. With very stringent system requirements, wireless communication systems play an important role in this scenery. For instance, Orthogonal Frequency-Division Multiplexing (OFDM) modulation (such as WLAN) and GSM systems require rigorous phase noise performance [1], which strongly depends on the resonator's Quality factor (a.k.a. Q factor) and power handling capability [2]. On-chip electrical resonators provided by conventional integrated circuit technologies can be inexpensive, but due losses from series resistance and substrate coupling [1], they suffer from prohibitively low Q factors [3]. Crystal resonators, in turn, can easily achieve high Q factors, but among off-chip components used in wireless communication systems, they are one of the most difficult devices to miniaturize and integrate on chip [2]. Combining both small size and high Q factor, over the past few years Micro-Electro-Mechanical System (MEMS) resonators has arisen as an interesting alternative [4]. As seen in [5], MEMS resonators can be integrated both monolithically or in the same package (SiP) [4], representing a drastic reduction in the overall system's footprint, and yet providing Q factors in the order of thousands [6] [7]. However, the design of a sustaining amplifier for oscillators employing MEMS resonators is not straightforward. Because of a typical high motional resistance (typically in the order of tens of kΩ [8]), to attend the Barkhausen criteria and achieve oscillation, the corresponding sustaining amplifier must present a high Gain Bandwidth Product (GBW). Boosted-gm regulated cascodes (RGC) [9] [8], for instance, is widely employed, but other topologies such as common-gate [10] and broadband current amplifiers [11] has also been reported. At last, MEMS resonators exhibit a very limited power handling capability when compared to a crystal's (usually a few $\mu$W - e.g. [12]), leading to a significant non-linear behavior even at low signal levels [2] [13]. In this case, the employment of an Automatic Gain Control (AGC) circuitry is strongly recommended, limiting the oscillation amplitude and hence decreasing the impact of the resonator's non-linearities on the system phase-noise performance [14]. Sections II and III describe the employed topology for both TIA and AGC circuitry, and preliminary simulation results are discussed. Finally, conclusions are made in Section IV. This TIA was realized in 0.18-um CMOS technology and is currently under fabrication.

## II. Transimpedance Amplifier

The block herein reported is a transimpedance amplifier designed with the purpose of oscillation sustaining for a MEMS-based oscillator. Described in Figure 1, the intended oscillator consists of a sustaining amplifier in closed-loop with a high frequency selectivity device (a MEMS resonator in this case)

Attenuating all components which are not the resonant frequency, the MEMS resonator combines a high Quality factor with a large motional resistance $R_S$, which can be lowered by either increase in transduction area (impacting in a higher contact parasitic capacitance - $C_{par}$) or bias voltage ($V_{bias}$) [13]. Therefore, for a better suitability, both TIA's terminals were decoupled ($C_{dec}$), so the resonator could be independently biased through a common bias tee.

To oscillate, as stated in [2], the system's sustaining amplifier must present a high transimpedance gain and wide bandwidth,

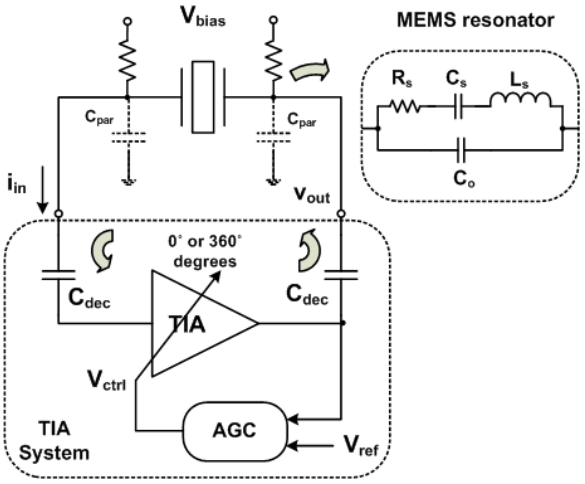


Fig. 1. General resonator-based oscillator. In this case, composed of a Variable Gain Transimpedance Amplifier (TIA) and AGC block in closed-loop with a resonator. In detail, the motional resistance (Rs), capacitance (Cs) and inductance (Ls) in parallel with a static capacitance (Co), comprising the equivalent RLC model of the MEMS resonator.

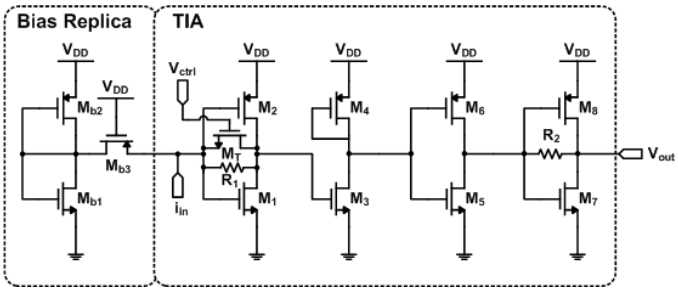


Fig. 2. TIA and Bias Replica

so negligible phase shift is observed around the resonant frequency. In other words, the TIA must provide enough gain to overcome the resonator's motional resistance (plus any other source of loss in the feedback loop) and all poles should be sitting at high frequencies. Considering a sizable contact parasitic capacitance ($\sim$1pF), it is therefore of great interest that both input and output impedances are made as low as possible, decreasing the input and output pole's impact on system's bandwidth, and also their loading effect on resonator's Q factor. Therefore, impacting on both system's bandwidth and resonator's Q factor, it is desirable that the proposed TIA presents a small input and output resistance.
Taking all the above mentioned into consideration, the topology seen in Figure 2 is proposed.

As noted, four inverter stages cascaded comprises the transimpedance amplifier. By proper dimensioning the output impedance of all inverter stages, each node had its time constant made low enough so the overall system's bandwidth could be optimized. Furthermore, by means of shunt-shunt feedback, both amplifier's input and output impedances were substantially lowered. The first stage's gain, defined by a triode feedback load ($M_t$), not only provides a low input impedance but also a wide gain tunability. In addition, a fixed resistance

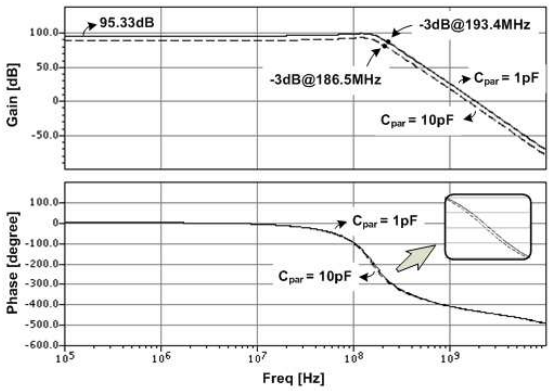


Fig. 3. Transimpedance gain and Phase versus Frequency. In detail, almost no phase shift is observed around -3dB frequency for both 1pF and 10pF parasitic capacitance

$R_1$ in parallel with $M_t$ is used to limit the amplifier's gain swing.
The remaining stages are fixed gain. With $M_4$ connected as diode, the second stage provides the necessary phase inversion with little impact on gain and bandwidth. The third and fourth stages, in turn, were designed to provide the remainder gain required by specification. Particularly, the output transistors $M_7$ and $M_8$ were made wide enough to confer the amplifier a low output impedance, combined with a large output swing, without excessively loading the third stage's output node with their gate-source capacitance. Considering both 2pF decoupling capacitors ($C_{dec}$), Figure 3 shows the maximum gain and phase shift for interconnection parasitic capacitance of 1pF and 10pF.

As observed, even for much higher parasitics, practically no difference is observed on bandwidth (only 3.5% decrease), stating that both input and output poles are isolated by the amplifier's low input and output impedances. For a 1pF parasitic capacitance, the respective -3dB bandwidth at maximum gain is 193.4MHz. Additionally, shown in Figure 4, the designed transimpedance amplifier provides a wide gain tuning range (53dB), making it suitable for oscillation sustaining with resonator's motional resistances ranging from 120Ω to 58 kΩ. If a minimum gain of 3 (three) is kept to ensure oscillation build-up, the upper limit drops to one third, corresponding to a still large tuning range of 43dB, approximately.
Considering a maximum phase shift of 10 degrees, for a 1pF parasitic capacitance, the highest resonant frequencies accommodated by the transimpedance amplifier are 13.2MHz and 20.1MHz for maximum and minimum gain conditions, respectively.

Additionally, all stages were made as scaled copies of the same inverter. By keeping the appropriate N-P ratio and scaling the finger number of each inverter stage, not only all internal nodes were designed to have the same bias voltage (at mid-rail), but every stage was properly dimensioned to present a good trade-off in gain, bandwidth, noise and power consumption. Moreover, when compared to boosted-gm Regulated

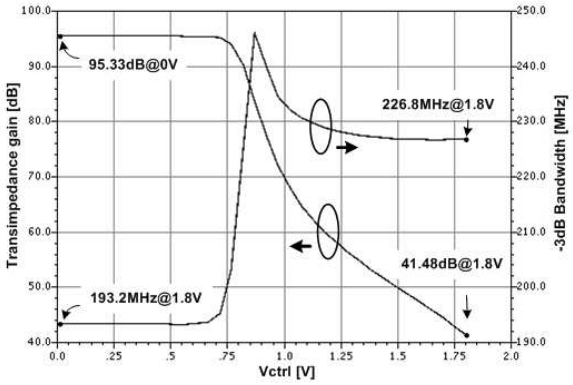


Fig. 4. Transimpedance gain and -3dB Bandwidth versus Control Voltage

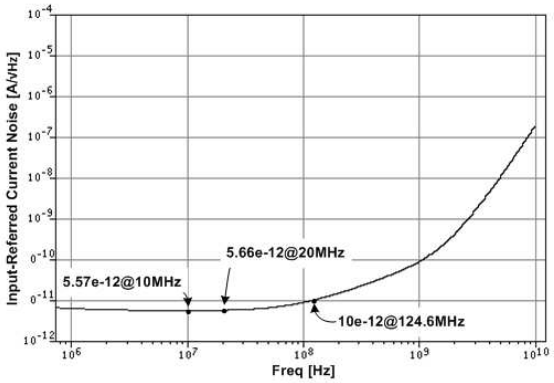


Fig. 5. Input-referred current noise

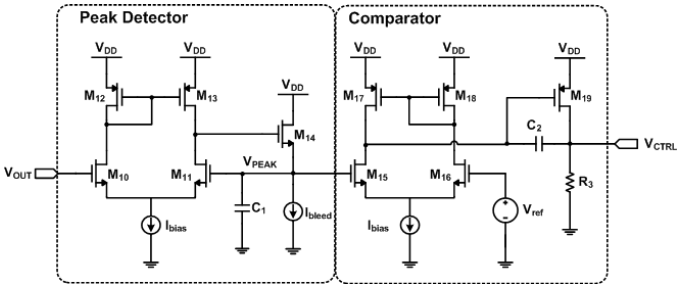


Fig. 6. Automatic Gain Control circuitry

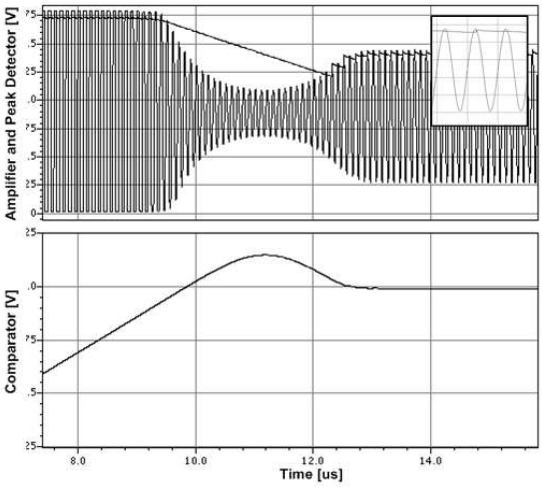


Fig. 7. Amplifier, Peak Detector and Comparator's output voltages. For a reference voltage of $V_{ref}$=1.4V, the obtained oscillation amplitude was only 50mV above the expected value

Cascode (RGC) amplifier, this topology has the advantage that any stage's noise contribution is directly coupled to the input node. As seen in Figure 5, a proper distribution of gain along the amplifier chain provides, at maximum gain, a input-referred noise of only 5.66pA/$\sqrt{Hz}$ at 20MHz.

Biased through a scaled replica in closed-loop [15], the transimpedance amplifier gains robustness and stability over PVT (Process-Voltage-Temperature) variations. Furthermore, for the applied topology, this technique allows that only one replica inverter is used to bias all other stages, decreasing both area and power consumption. After layout, with pads excluded the whole amplifier has occupied a total area of 0.018mm$^2$, and the power consumption is expected to be around 3.2 mW from a 1.8V supply.

## III. Automatic Gain Control

As previously mentioned, because of a limited power handling capability of the MEMS resonator, an Automatic Gain Control (AGC) circuit was implemented. Shown in Figure 6, this topology is widely applied [2] [16] and comprises a peak detector to sample the oscillation amplitude, followed by a comparator.

The peak detector consists of a peak rectifier with a MOS transistor ($M_{14}$) in the feedback path. Attached to the output, a MOS capacitor ($C_1$) samples the peak value while a bleeding current discharges it. In few words, when $V_{out}$ is higher than $V_{peak}$, $M_{14}$ is turned ON and the sampling capacitor is charged until $V_{peak}$ equals $V_{out}$. On the other hand, when $V_{peak}$ is higher than $V_{out}$, $M_{14}$ is OFF and the sampling capacitor is discharged at a constant rate, allowing the peak detector to rapidly track any amplitude variation.

The comparator, in turn, was implemented as a simple over-compensated two-stage operational amplifier. By addition of a 10pF compensation capacitor the amplifier is very limited in bandwidth, presenting a very low frequency dominant pole. It is important to notice that since power-up conditions push $V_{ctrl}$ to zero, maximum gain will be available for oscillation start-up. Figure 7 shows the open-loop behavior of the sustaining amplifier.

As noted, the system is able to rapidly track the oscillation amplitude set by $V_{ref}$. The overshooting effect is due a large sampling capacitance ($C_1$), dimensioned to operate with a wide range of oscillation frequencies. In detail, both peak detector and amplifier's output voltages. Provided it's large output swing capability, the proposed topology provides a reduced distortion of the output signal, with a simulated THD of only 2.69%.

## IV. Conclusion

The reported design has been implemented using a fully CMOS compatible technology and is currently under fabrication. As observed, the proposed topology is capable of achieving a high transimpedance gain with reduced power and area consumption. Nonetheless, the reported TIA provides a wide gain tunability of 53dB$\Omega$, with both low input and output impedances, making it suitable for a wide range of MEMS resonators with different combinations of motional resistances and interconnection parasitic capacitances. At last, the obtained low input-referred current noise of 5.66pA/$\sqrt{Hz}$ paves the way for a good phase noise performance resultant oscillator.

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